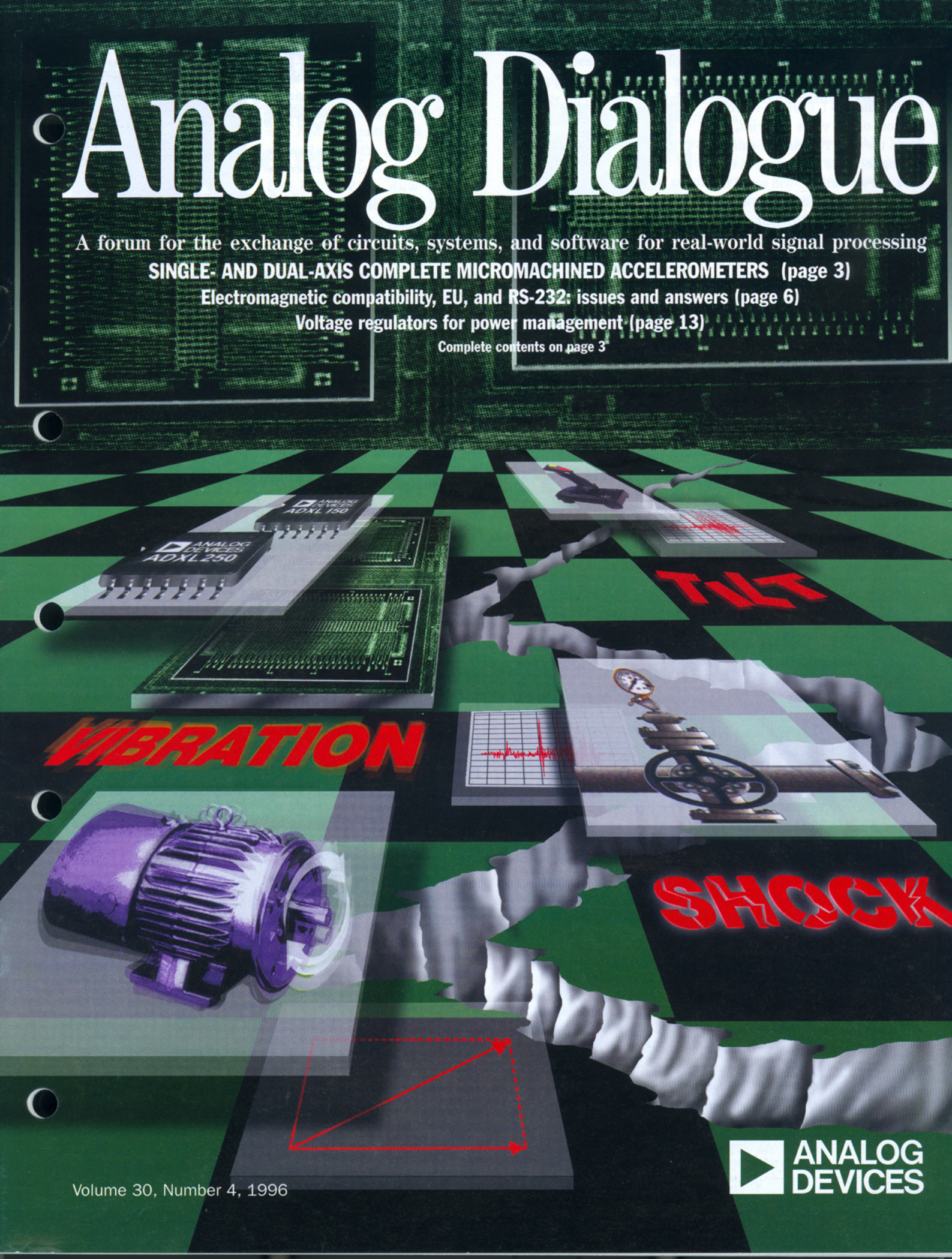
Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing



Volume 30, Number 4, 1996

ANALOG DEVICES

Editor's Notes

THIRTY YEARS OF ANALOG DIALOGUE

In Volume 15-1 (1981), in celebration of 15 years in print, we listed the first 15 years of Analog Dialogue cover features. At that time, we wrote: ". . . will mark the 15th year of publication of this journal, and the 13th year of our stewardship. While adding a copy of the [most recent] issue to our bulging binder, we nostalgically turned the pages of issues long forgotten. The amount of technological progress reported in them surprised even us. Before the list expands beyond the capacity of this column, we thought you might be interested in seeing a roll of just the cover stories alone, though much significant progress never attained the cover." In this spirit, in celebration of our 30th year in print (and 28th of stewardship), here are the second 15 years of cover themes:

1981 15-2 *D/A converters for graphic displays*
1982 16-1 *High-performance hybrid-circuit isolation amp* (AD293)
16-2 *Dual monolithic multiplying DACs* (AD7528)
16-3 *Monolithic instrumentation amplifier* (AD524) *and thermocouple preamp* (AD594)
1983 17-1 *CMOS ICs for digital signal processing*
17-2 *Quad CMOS DAC with buffered voltage outputs*
1984 18-1 *Amplifier noise basics revisited*
18-2 *Monolithic V-out µP-compatible 12-bit DAC* (AD667)
18-3 *An intelligent vision system for industrial image analysis*
1985 19-1 *Multifunction analog IC computes $y(z/x)^m$, etc.* (AD538)
1986 20-1 *Low-cost, high-performance, compact iso amps* (AD202/4)
20-2 *Fast, flexible CMOS DSP µP* (ADSP-2100)
1987 24-1 *Monolithic process-control transmitters* (AD693)
21-2 *Complete 8-bit 400-ksps analog I/O* (AD7569)
1988 22-1 *Chipset for 50-Mbit/s digital data recovery* (AD890/891)
22-2 *200-MSPS 8-bit IC ADC with 250-MHz BW* (AD770)
1989 23-1 *Isolated sensor-to-serial with a screwdriver* (6B Series)
23-2 *Single-chip DSP microcomputer* (ADSP-2101)
23-3 *DC-120-MHz IC log amp—accurate compression* (AD640)
23-4 *Pin electronics for high-speed ATE* (AD1315/1521/22)
1990 24-1 *Monolithic 75-MSPS 10-bit flash converter* (AD9060)
24-2 *Mixed-signal processor: DSP/ADC/DAC* (ADSP-21msp50)
24-3 *RAM-DAC upgrade enhances VGA graphics* (AD7148)
1991 25-1 *Pro-Logic decoder: Dolby "Surround Sound"* (SSM2125)
25-2 *ADSP-21020 floating-point high-speed DSP*
1992 26-1 *Mixed-signal chips drive digital radio* (AD7001/7002)
26-2 *Wideband "linear in dB" VCA* (AD600/602)
1993 27-1 *Fast precise 155-Mbps fiberoptic timing recovery* (AD802)
27-2 *Single-chip micromachined accelerometer* (ADXL50)
1994 28-1 *Dual-setpoint single-chip temperature controller* (TMP01)
28-2 *Complete, low-distortion 500-MHz IC mixer* (AD831)
28-3 *SHARC Floating-point DSP: tops in memory, performance*
1995 29-1 *Integrated stereo codecs for multimedia* (AD1843/1845)
29-2 *Meeting the challenges of high speed*
29-3 *Considerations in low-power, single-supply system design*
1996 30-1 *Read-channel processor uses PRML with MR heads*
30-2 *DSP-based chip set for ac motor control* (ADMC201)
30-3 *CMOS DACs optimized for transmit path* (AD976x family)
30-4 *Dual-axis accelerometer* (ADXL250) A

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[*More authors on page 22*]

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Single- and Dual-Axis Micromachined Accelerometers

ADXL150 & ADXL250: New complete low-noise 50-*g* accelerometers

by Howard Samuels

The ADXL150 and ADXL250 represent the newest generation of surface-micromachined monolithic accelerometers* from Analog Devices. Like the landmark ADXL50 (*Analog Dialogue* 27-2, 1993), the new devices include both the signal conditioning circuitry and the sensor, fabricated together on a single monolithic chip—providing acceleration measurement at very low cost with high reliability. As with the ADXL50, the sensor structure is a differential capacitor, but it is modified to take advantage of the experience gained from producing millions of ADXL50s, further advancing the state of the art of micromachined sensor design.

The sensor: The silhouettes in Figure 1 compare the sensors used in the ADXL50 and the ADXL150. Both sensors have numerous fingers along each side of the movable center member; they constitute the center plates of a paralleled set of differential capacitors. Pairs of fixed fingers attached to the substrate interleave with the beam fingers to form the outer capacitor plates. The beam is supported by tethers, which serve as mechanical springs. The voltage on the moving plates is read via the electrically conductive tether anchors that support the beam.

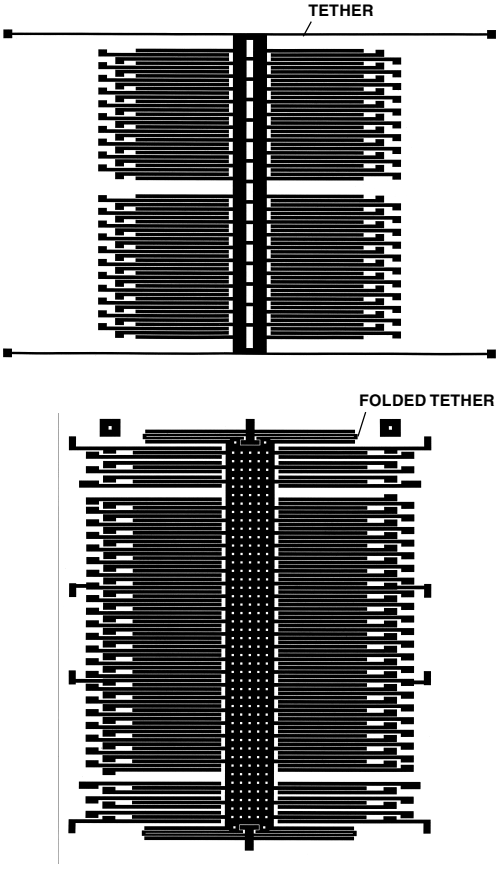

Figure 1. Silhouette plots of ADXL50 (upper) and ADXL150 (lower). Axis of motion is vertical.

*For technical data, visit our Web site, http://www.analog.com. Data is also available in North America around the clock by Analogfax™, 1-800-446-6212; request **2060**; or use the reply card. **Circle 1**

The polysilicon support springs (tethers) are highly reliable. Many devices have been tested by deflecting the beam with the equivalent of > 250× the force of gravity, for > 7×10^{10} cycles, with zero failures, as part of the product qualification process.

The ADXL50's tethers extend straight out from the beam in an 'H' configuration. On the ADXL150, however, the tethers are folded, reducing the size of the sensor and halving the number of anchors (Figure 2). Since each anchor adds parasitic capacitance, the smaller number of anchors reduces capacitive load, increasing the sensor's acceleration sensitivity. In addition, the tether geometry minimizes sensitivity to mechanical die-stress; this allows the ADXL150 to be packaged in standard cerdip and surface-mount cerpak packages, which require higher sealing temperatures (and associated thermal stress) than metal cans. The folded tether was first used in the ADXL05 low-*g* accelerometer; its higher sensitivity makes die stress more of a concern.

In addition to the *sense* fingers projecting from both sides of the beam, the ADXL150 has 12 *force* fingers (visible near both ends

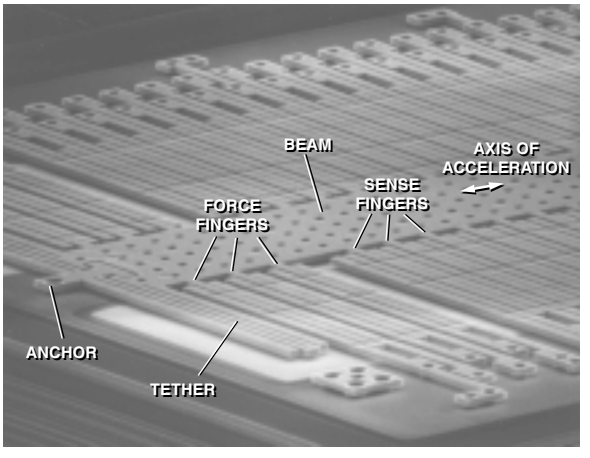

Figure 2. Partial aerial SEM view of one end of the ADXL150's sensor.

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of the beam), used for self-test actuation. The plates of a parallel-plate capacitor attract each other with an electrostatic force of:

$$F = \frac{\varepsilon A V^2}{2d^2}$$

where ε is the permittivity of the material between the plates, A is the area of the plates, V is the voltage across the capacitor, and d is the distance between the plates.

In normal operation, the fixed fingers on either side of the force fingers are at the same voltage potential as the beam and its fingers. With no voltage between the force fingers on the beam and the fixed fingers on the substrate, there is no electrostatic force. However, when a digital self-test input pin is activated, the fixed fingers on one side of the force section are driven to a nonzero dc voltage, applying a force to the sense fingers, deflecting the beam. The forcing voltage is laser-trimmed to produce a net electrostatic force on the beam equivalent to a 10-*g* acceleration. This voltage will depend on the specific electrical and mechanical characteristics of each individual device.

The self-test circuitry operates independently of the normal accelerometer signal path. When self-test is activated, the deflection it produces is measured by the device in the same way as a deflection produced by accelerating the entire device. Since the full-scale deflection of the sensor is only about 1.5% of the gap between the capacitor fingers, the self-test response is nearly constant, adding to the deflection caused by any existing acceleration. Like an externally applied acceleration, the deflection produced by the self-test circuitry makes full use of the measurement circuitry of the normally functioning accelerometer to generate an output, so it is a highly reliable indicator of the device's ability to function correctly.

Circuit Architecture: As Figure 3 shows, the fixed fingers are driven with antiphase square waves. Unlike the ADXL50, which uses a dc bias between the excitations and the beam as a means of providing a force-balance feedback path, the ADXL150 employs an open-loop architecture. With zero average dc voltage on the beam, the excitation square waves can swing to the power supply rails, with the beam biased at one half the supply voltage. The larger amplitude of the 100-kHz excitation in the ADXL150 results in reduced sensitivity to electronic device noise and is a contributing factor to its improved noise performance.

If the beam is perfectly centered, both sides of the differential capacitor have equal capacitance, and the ac voltage on the beam is zero. However, if the beam is off center due to an applied acceleration (or self-test deflection), the differential capacitor becomes unbalanced. The beam waveform is a square wave with amplitude proportional to the amount of displacement, and hence, acceleration magnitude. The phase of the beam voltage relative to the excitation determines the acceleration polarity.

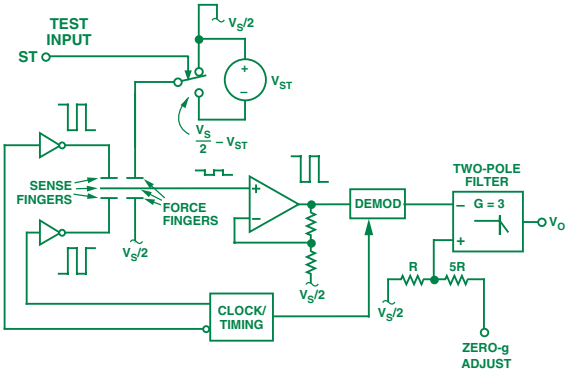


Figure 3. ADXL150 electrical block diagram.

The beam output is connected directly to a noninverting amplifier, which provides buffering for the high impedance beam node, as well as gain for the 100-kHz output signal.

The output is demodulated in a synchronous demodulator that samples the amplifier output after it has settled in each half of the excitation cycle. By detecting the difference between the amplifier's output levels for the two states, the offset voltage of the amplifier is eliminated, much like that of a chopper stabilized amplifier. Since the demodulator is phase synchronized with the excitation, the output signal polarity correctly indicates the direction of the applied acceleration.

The ADXL150 has a 2-pole gain-of-3 Bessel low-pass filter on board [the ADXL250—see below—includes a 2-pole filter for each channel]. These filters can be used to prevent aliasing of high-frequency components in the demodulator output with A/D converter clock frequencies in associated data-acquisition circuitry. A second input to the filter is connected to a resistive divider with a gain of 1/6, brought out to a package pin. It provides a convenient offset adjustment point for the accelerometer, with a net gain of +0.5 for the applied voltage.

Because extensive use is made of CMOS logic, and the open-loop architecture allows simpler signal conditioning circuitry, the device draws only 1.8 mA of supply current at 5 V (including the 2-pole output filter), a >80% reduction from the ADXL50.

The increased excitation levels used, along with carefully executed chopper modulation/demodulation techniques, yield a noise density of just 1 m$g/\sqrt{\text{Hz}}$, less than 1/6 that of the ADXL50. The improved dynamic range enables the ADXL150 to be used in applications such as machine health, vibration monitoring, shock sensing, and instrumentation.

The ADXL150 has a sensitivity of 38 mV/*g*, measured at the output pin. The full scale range is ±50 *g*, for a total signal swing of 3.8 V, with a single 5-V supply. This significant output voltage range allows the designer to take full advantage of the input range of a single-supply A/D converter, such as might be found in a microprocessor system.

The output voltage is given by the relationship:

$$V_O = V_S\left(\frac{1}{2} + \frac{\alpha \cdot 0.038\ \text{V}}{5\ \text{V}}\right)$$

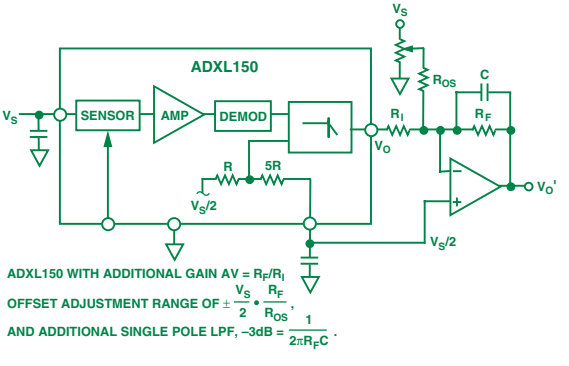


Figure 4. ADXL150 with an external op amp for additional gain and filtering.

α is the applied acceleration expressed in gs (1 $g \approx 9.8$ m/s^2), and V_S is the power supply and reference voltage, nominally 5 V. If V_S is also used as the reference for a ratiometric A/D converter, the system will reject variations in V_S. With zero applied acceleration, the output of the ADXL150 is $V_S/2$, which is half scale of the A/D converter. Even if V_s is not exactly 5 V, the digital output code of the A/D converter still reads half scale. For any applied acceleration, the output of the A/D converter will be essentially independent of changes in V_S.

Without external manipulation of the filter's offset, the device provides a convenient reference point at one half the power supply voltage. An external operational amplifier can be used (Figure 4), for additional gain with respect to this voltage to increase the sensitivity of the accelerometer. An additional external capacitor can be used in this circuit to add a third pole after the internal two-pole filter. The offset can be adjusted by current injected into the summing node of the external amplifier.

The ADXL250 adds a new dimension: The ADXL250, a single monolithic chip (Figure 5), measures both the x and y coordinates of acceleration in a given plane (e.g., forward-back and side-to-side). Because the sensitive axis of the ADXL150's sensor is in the plane of the chip, twin sensors can be fabricated on the same die, with one rotated 90 degrees from the other. The ADXL250 is the world's first commercially available two-axis monolithic accelerometer.

Both channels share the clock generator, demodulator timing, self test logic, and bias voltage. Each sensor receives the clock signals via its own CMOS inverter drivers, and the signals generated by the sensors are treated completely independently.

The single self-test pin activates both sensors simultaneously, simplifying the interface to a microprocessor. As in the ADXL150, the test signal deflects each sensor by an amount equivalent to a 10-g acceleration. Each channel has its own offset adjustment pin and its own output voltage pin. Both channels have the same sensitivity.

The total power-supply current of the two-channel ADXL250, is typically 3.5 mA (5 mA maximum, including the output filters—just half the typical supply current of the earlier ADXL50). Both devices have A and J versions, specified for temperature ranges –40 to +85°C and 0 to +70°C. Prices (100s) start at $12.45 (ADXL150JQC) and $19.95 (ADXL250JQC).

How do I use them? The ADXL150 is a complete sensor on a chip. Just connect a single 5-V power supply (with clean output, bypassed to ground by a decent-quality ceramic capacitor) and connect the output to its readout destination.

If the self-test pin is left open-circuited, an internal pulldown resistor ensures normal operation. With nothing connected to the offset adjust pin, the output voltage is unmodified.

To adjust the output zero-g voltage level, use the offset adjust pin. The offset can be adjusted by applying an analog dc voltage, including the supply voltage or ground. Computer control can be achieved in various ways, e.g., by a serial or parallel D/A converter, or by a modulated duty cycle with an R-C averager. A choice of three offset adjustment values can be achieved with a three-state digital output bit and a series resistor.

The ADXL150 and ADXL250 were developed by multidisciplinary product teams in ADI's Micromachined Products Division, Wilmington, MA. A

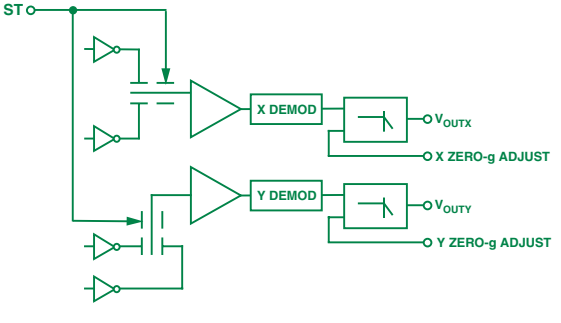
MOUNTING AND MECHANICAL CONSIDERATIONS

When an accelerometer is mounted on a PC board, the IC becomes part of a larger mechanical system. Accelerations of 50 g cause the sensor to deflect within the IC package; in addition, the PC board and its mounting structure will deflect and deform. The motion of the board generates a false acceleration signal, which the accelerometer can sense. If the resonant frequency of the supporting structure is within the signal band or not much higher than the filter rolloff, the vibrations of the PC board and its mounting system will show up in the sensor output.

The best way to minimize these effects is to make the mounting scheme as stiff as possible, thereby transmitting the system acceleration more faithfully to the sensor and increasing the resonant frequency. Since a PC board is much stiffer in its plane than perpendicular to its surface, the accelerometer's sensitive axis (both axes, if dual) should be in the plane of the board.

Because the ADXL150 and ADXL250 have their sensitive axes in the plane of the chip, and the surface of the chip is parallel to the base of the package, the accelerometers receive the benefit of the PC board's stiffness when simply soldered to the board.

If the sensitive axis were perpendicular to the plane of the chip (as is the case for some bulk-micromachined sensors), soldering the package to the board would render the measurement most susceptible to PC-board flexibility. A right-angle mounting system could be used to orient the sensitive axis parallel to the PC board, but the mounting system itself can deform, producing false acceleration readings. The mounting system, and any PC board stiffeners, add cost to the acceleration measurement. Also, the additional mass of the mounting system lowers its resonant frequency, causing larger false acceleration signals.



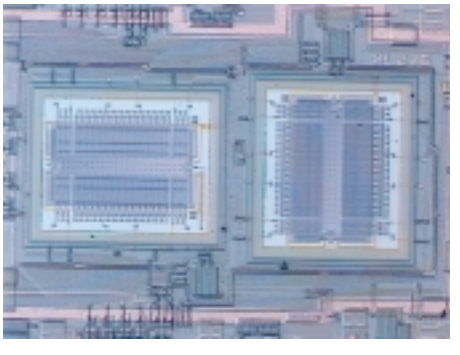


Figure 5. ADXL250 block diagram (L) and partial chip photo showing sensors at right angles in plane of chip (R).

EMC, CE Mark, IEC801 .....What's it all about?

And new devices to ease the job

by Matt Smith

This article examines **electromagnetic compatibility** (EMC), which has assumed increased formal significance since January, 1996. We discuss here the special requirements and standards that are mandatory for all pieces of equipment entering the market in the European Union (EU), and we consider the requirements for attaining the "CE" *(Communauté Européene)* mark from an EMC point of view. A new generation of RS-232 products, designed to meet these requirements, exemplifies the measures that have been taken by Analog Devices to achieve EMC at the IC level. These measures include inbuilt protection circuitry to provide levels of immunity far beyond anything previously available; immunity to *electrostatic discharges* (ESD) in excess of 15 kV has been achieved—measured by new and more-stringent test methods. We also discuss protection against overvoltage and *electrical fast transients* (EFT). From the *emissions* point of view, we examine electromagnetic emissions and the measures we have taken in ICs to eliminate costly shielding procedures.

The European Union EMC Directive: In May, 1989, the European Union published a Council Directive, 89/336/EEC, relating to electromagnetic compatibility of products placed on the market within the member states. A later amendment, 92/31/EEC, delayed compulsory compliance until January 1, 1996. The Directive applies to apparatus which is liable either to cause electromagnetic disturbance or itself be affected by such disturbance—and thus to all electrical or electronic products. It goes beyond the more familiar FCC Class B requirement for emissions control since it also addresses *immunity* as well as emissions. While the directive applies only to products marketed within the EU, the standards are likely to be adopted worldwide.

Conformance with the EU Directive on Electromagnetic Compatibility requires that products will

- Have high intrinsic immunity to emissions from other sources
- Keep their undesirable emissions to within very strict limits

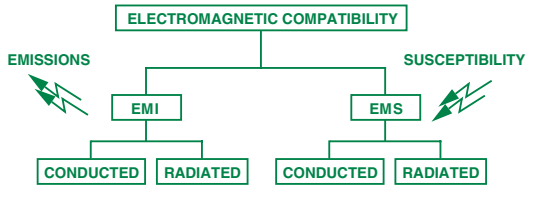
Manufacturers are responsible for meeting the regulations; from January 1, 1996, all electronic products sold in the European Union *must* show conformance by displaying the CE mark.

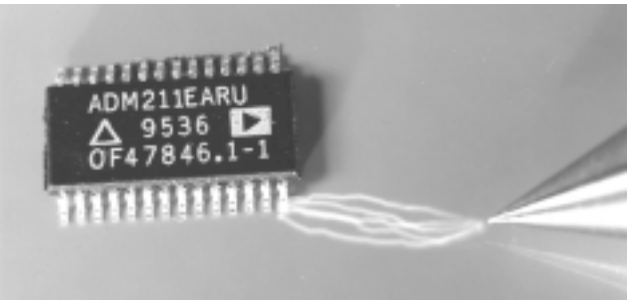
Definitions:

Electromagnetic compatibility (EMC): Ability to operate in, and not overly contribute to, an environment of electromagnetic radiation. When this goal is met, all electronic equipments operate correctly in one another's presence.

Electromagnetic interference (EMI): Electromagnetic energy emanating from one device causing degraded performance in another.

Electromagnetic immunity, or *susceptibility* (EMS): Tolerance of the presence of electromagnetic energy.





EMC Testing: Thorough EMC evaluation requires testing of both EMI and EMS. Requiring different measurement approaches and test methodologies, they are specified in separate Standards. *Emitted* energy may be *conducted* via the power supply lines or on I/O cables, or it may be *radiated* through space. It can start out by being conducted along cables and then be radiated when shielding is inadequate. Similarly, electromagnetic immunity, or *susceptibility*, must be tested for both conducted and radiated interference. Conducted interference includes *electrostatic discharges* (ESD) and *electrical fast transients* (EFT).

Emissions testing is not new, but only now has *immunity* testing become mandatory on commercial products—a result of the EU regulations. The standards for commercial immunity testing, both conducted and radiated, have evolved over several years

IEC1000-4-x Immunity Specifications: The basic EMC immunity standards in Europe come from the International Electrotechnical Commission (IEC). The content and document numbers have continually evolved over many years. In the latest round, the IEC have assigned IEC1000-4-x to the family of immunity standards previously known as the IEC801-x series. For example, the specification dealing with ESD immunity, previously referred to as IEC801-2, has become IEC1000-4-2.

Nomenclature	Subject
IEC1000-4	Electromagnetic Compatibility EMC
IEC1000-4-1	Overview of Immunity Tests
IEC1000-4-2	Electrostatic Discharge Immunity (ESD)
IEC1000-4-3	Radiated Radio-Frequency Electromagnetic Field Immunity
IEC1000-4-4	Electrical Fast Transients (EFT)
IEC1000-4-5	Lightning Surges
IEC1000-4-6	Conducted Radio Frequency Disturbances above 9 kHz

EMC AND I-O PORTS

It has been estimated that up to 75% of EMC problems occur in relation to I-O ports. The I-O port is an open gateway for electrostatic discharges or fast transient discharges to enter a piece of equipment, and for interfering signals to escape, either by conduction of spurious signals on the I-O lines or by radiation from the I-O cable. Because of this, the EMC performance of the I-O transceiver device connected to the port is crucial to the EMC performance of the entire package.

Electromagnetic Susceptibility of I-O Ports: I-O ports are particularly vulnerable to damage from EMI because they may be subjected to various forms of overvoltage during "normal" operation. Simply plugging or unplugging cables carrying static charges can destroy the transceiver. RS-232 serial ports are especially vulnerable A standard serial port uses an exposed 9-way male D connector. The pins on the connector are all too easily accessible, making them a prime target for accidental discharges. ESD damage can result from simply picking up a laptop PC after walking across a carpeted room.

The traditional method for ensuring immunity against ESD on I-O ports, including RS-232, has been to use some form of voltage clamping structure such as Tranzorbs, or current-limiting resistors. Damage to an integrated circuit is caused by excessive current flow, usually induced by high voltages. Protection can be achieved using *current diversion* or *current limiting.*

Current Diversion: An integrated circuit may be protected by diverting some of the current to ground externally, usually with a structure that provides voltage clamping. The voltage clamp must switch on quickly and be able to safely handle the current that it is diverting away from the IC. Tranzorbs are a popular choice, but they are expensive and space consuming. For example, an RS-232 port has eight I-O lines, each requiring individual protection; the protection components can often take up more area than the transceiver itself. In today's laptop computers, where both costs and board space must be minimized, this is far from ideal. Another disadvantage of external clamping structures is their heavy capacitive loading on the I-O lines. This limits the maximum data rate, and the charging/discharging on data edges contributes to battery drain—another serious drawback in portable equipment.

Current Limiting: Current-limiting protection using simple series resistors is a popular choice where the overvoltages likely to be encountered are relatively low. But for ESD protection, where the voltages can be as high as 15 kV, it is not a feasible option. The resistance value required to keep the current within safe limits (200 mA or so) would be so high as to defeat normal operation of the transceiver. Other current limiting components such as thermistors are occasionally used; but again, protection is achieved at the expense of output impedance. Current limiting is often used in combination with voltage clamping to achieve a good compromise, giving high levels of protection but without degrading normal operating specifications. Still, the external structures are undesirable in portable, low-cost equipment.

EMC Emissions on I-O ports: One might not think of RS-232 ports as likely offenders since the data rates are quite modest. But emissions are indeed a concern, and for a number of reasons.

In recent years, transmission speeds have been pushed up by a factor of 10 over the originally intended RS-232 speeds. The now-common V.34 modems require data rates in excess of 115 kbps. Higher speed modems are now appearing, pushing the rate up to 133 kbps. ISDN pushes this even higher—up to 230 kbps . Higher frequencies, together with high voltages, translate into higher levels of emissions. The move towards single-supply, charge-pump-based transceivers has resulted in on-chip high-frequency clock oscillators. The latest generation of charge-pump-based products uses 0.1-µF charge-pump capacitors in order to conserve board space, but at the price of higher oscillator frequencies, resulting in higher levels of emissions. The high voltage switching (20 V), high frequencies, and the driving of long, often unshielded cables are a recipe for EMI trouble unless great care is taken. The RS-232 cable serves as a very effective antenna, and even low level noise coupled onto the RS-232 cable can radiate significantly.

"FIXES" vs. PREVENTION

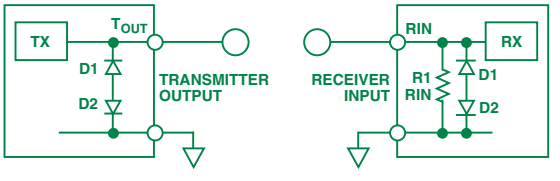
Too often, EMC problems are discovered late in a product design cycle and require expensive redesign including shielding, additional grounding, voltage-clamping structures, etc. Such "Band-Aid" fixes can be time- and space consuming, expensive, and lacking in guarantees of success. It helps to understand and eliminate potential EMI problems, both emissions and immunity, as early as possible in the design cycle.* It will be helpful to include, where possible, products that have already been tested for compliance and characterized so you know just how close to the limits you are running.

The ADM2xxE family† of RS-232 interface transceiver products (*Analog Dialogue* 30-3, p. 19) is an example of devices that have been designed with EMC compliance as an important consideration. High levels of inherent immunity to EMI as well as low levels of radiated emissions make for fewer headaches for the system designer. Benefits include low cost, space saving, inbuilt ruggedness and low emissions.

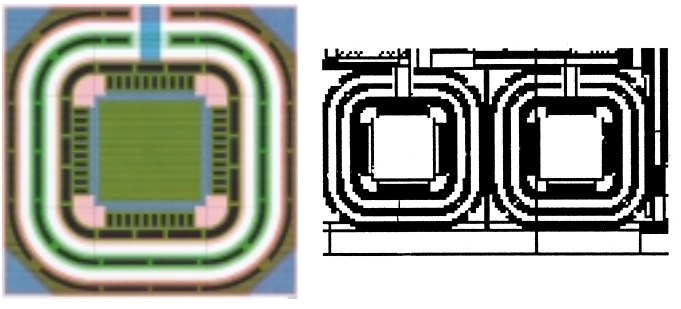
On-chip immunity: On-chip ESD, EFT and EMI protection structures ensure compliance with the requirements of IEC1000-4-2, IEC1000-4-3 and IEC1000-4-4. All inputs and outputs are protected against electrostatic discharges up to ±15 kV, and electrical fast transients up to ±2 kV. This ideally suits the devices for operation in electrically harsh environments or where RS-232 cables are frequently being plugged or unplugged. They are also immune to high R-F field strengths (1000-4-3), allowing operation in unshielded enclosures.

All this inherent protection means that costly external circuitry can be eliminated, saving cost and board space; fewer components means increased system reliability; and data-transmission speed, often compromised by external protection, is maintained.

Protection Structure: A simplified version of the protection structure used is illustrated below. It basically employs two back-to-back diodes. Under normal operating conditions, one or the other of these diodes is reverse-biased. If the voltage on the I-O pins exceeds ±50 V, reverse breakdown occurs and the voltage is clamped, diverting the current through the diodes. Two diodes are required because the RS-232 signal lines are bipolar , usually swinging from –10 V to +10 V. The transmitter output and receiver input use the same protection structure. The receiver input's terminating 5-kΩ resistor also aids in current diversion.



The diodes must be capable of dissipating the energy present in ESD pulses. They must be able to switch at high speed, safely dissipate energy, and occupy minimal die area. The diagram below, which illustrates how this was achieved, is the actual structure



*See "A bibliography on EMC/EMI/ESD", *Analog Dialogue* 30-2 (1996). **Circle 2**

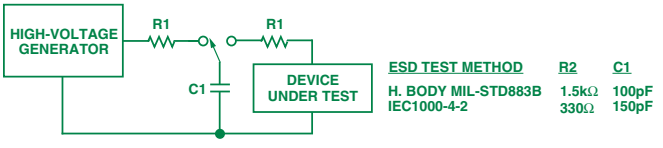
†For technical data, visit our Web site, http://www.analog.com. Data is also available in North America around the clock by Analogfax™, 1-800-446-6212; request **1992** and **1991**; or use the reply card. Circle **3**

used for receiver input and transmitter output. The annular structure around each pad embodies the P-N junction, achieving optimum charge distribution with minimum die area.

Testing ESD Protection to IEC1000-4-2: This structure meets the test requirements of IEC1000-4-2, which are much more stringent that the more usual MIL-STD-883B or human body model test. Such traditional ESD test methods, used by most semiconductor manufacturers, were intended to test a product's susceptibility to ESD damage during handling and board manufacture. They do not adequately test a product's susceptibility to real-world discharges. Each pin is tested with respect to all other pins, simulating the types of discharge likely to occur during handling or with auto insertion equipment. There are important differences between these tests and the IEC test.

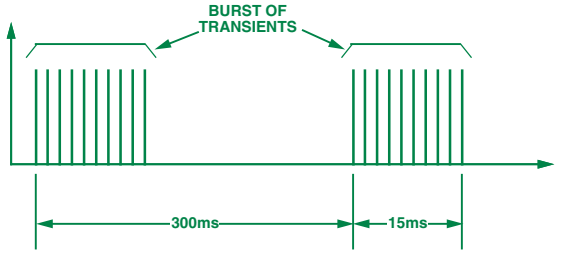
IEC1000-4-2 vs. MIL-STD-883B: The IEC test is much more stringent in terms of discharge energy. Shown below is a simplified schematic of the ESD test generator. Capacitor C1 is charged up to the required test voltage via R1. The energy in C1 is then discharged into the device under test via R2. The peak current and discharge energy are determined by R2 and C1. The table shows that for the IEC test, R2 is decreased from 1.5 kΩ to 330 Ω, resulting in a >4× peak current increase. In addition, C1 is increased by 50% from 100 pF to 150 pF. Furthermore, the IEC1000-4-2 test, applied to the I-O pins, is carried out while power is applied to the device, to check for potential destructive latchup, which could be induced by the ESD transient.

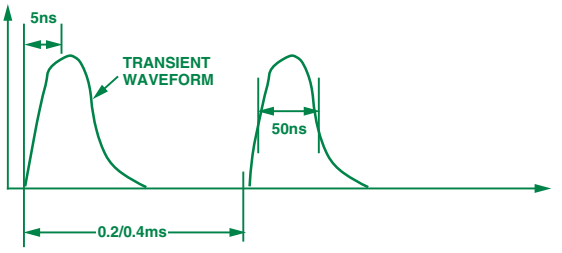
The IEC test therefore better represents a real-world I-O discharge where the equipment is operating normally with power applied. But for maximum peace of mind, both tests should be performed to ensure maximum protection during both handling and manufacture, as well as later during field service.



ESD TEST METHOD	R2	C1
H. BODY MIL-STD883B	1.5kΩ	100pF
IEC1000-4-2	330Ω	150pF

IEC1000-4-4 (previously IEC801-4) Electrical Fast-Transient Immunity: Electrical fast transients occur as a result of arcing contacts in switches and relays. The tests defined in IEC1000-4-4 simulate the interference generated when, for example, a power relay disconnects an inductive load. An arc is produced, due to the high back EMF (Ldi/dt). Because of contact bounce as the switch is opened, the arc is actually a burst; therefore, the voltage appearing on the line consists of a burst of extremely fast transient impulses. The fast-transient burst test defined in IEC1000-4-4 attempts to simulate the interference resulting from this type of event with the waveforms shown here.





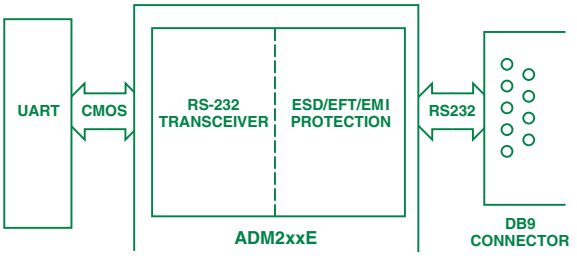
The waveform consists of a 15-ms burst of 2.5- to 5-kHz transients repeated at 300-ms intervals. These transients are coupled onto the I-O lines using a 1-meter capacitive clamp. Voltages as high as 2 kV are applied with the fast transition times shown. This can either destroy an unprotected IC connected to the I-O line immediately or cause degradation in performance with delayed failure. The protection scheme described above, used for the ADM2xxE, clamps the overvoltages to a safe level

IEC1000-4-3 (previously IEC801-3) Radiated Immunity: This specification describes the measurement method and defines the levels of immunity to radiated electromagnetic (EM) fields. It was originally intended to simulate the EM fields generated by sources such as portable radio transceivers, that generate continuous-wave radiated EM energy. Its scope has since been broadened to include spurious EM energy, which can be radiated from fluorescent lights, thyristor drives, inductive load, etc.

In tests for immunity, the device is irradiated with an EM field in one of a variety of ways. Integrated circuits are conveniently tested using some form of *stripline cell*, which consists of two parallel plates with an electric field developed between them. A high-power RF amplifier generates the field, which is swept in frequency from 80 MHz to 1 GHz. The device under test is placed within the cell and exposed to the electric field. A field-strength monitor within the cell provides feedback to maintain a constant field level as the frequency changes. Three severity levels are defined, with field strengths from 1 to 10 V/m. Results are classified in a similar fashion to those for IEC1000-4-2.

Emissions: EN55 022, CISPR22 defines the permitted limits of radiated and conducted interference from information-technology (IT) equipment. The objective of the standard is to minimize both types of emissions, such as are produced by switching circuits that involve switching current at high frequencies. For ease of measurement and analysis, conducted emissions are assumed to predominate below 30 MHz, radiated emissions above 30 MHz.

The best and easiest method of minimizing emissions is to reduce them at the source; for example, the charge-pump design used in the ADM2xxE family has a major objective of minimizing switching transients without any additional filtering or shielding components. This eases the system designer's task, saves cost and space by eliminating external filters and other high-frequency suppression or shielding elements, and completely avoids filtered connectors, often an expensive last resort. A



Advanced Digital Video Encoders

CCIR-601 YCrCb to NTSC/PAL: studio quality digital video at consumer video prices

by Bill Slattery

The ADV7175/ADV7176* digital video encoders convert digital video data into standard analog baseband (NTSC/PAL) television signals. These low-cost, high-performance devices encode digital YUV (CCIR-601/656—4:2:2) and square pixel component video; and they can drive EuroSCART (RGB), S-Video (Y/C) and YUV analog video signals, as well as supporting closed-captioning and Teletext. The AD7175 also includes Macrovision® antitaping (license required from Macrovision, Inc.) The digital input section interfaces gluelessly to all standard MPEG (1 & 2) Decoders. Applications encompass TV settop boxes, VideoCD, DVD, Internet/Network Computers, Web TVs and Multimedia PC Video, as well as professional broadcast/studio video equipment. Packaging in a tiny 44-Lead PQFP. Prices (10,000) start at $7.59.

Digital video: Television signals are, in the main, transmitted in standard analog format; the signal is received over an outdoor or indoor antenna, or over a cable distribution system that may have a local analog settop box to enable pay-TV channels. This system, based on the composite analog NTSC (North America, Japan) and PAL (Europe) formats, has existed for 40 years or more and has served consumers quite well worldwide. Recently, however, television broadcasting has undergone revolutionary changes. Intent on permitting existing equipment and program material to continue in use, broadcasters have had to maintain backward compatibility of the existing format but transmit and distribute it with digital processing. Analogous to the evolution from black-and-white TV to color TV, this change will allow complete backward compatibility and transparency for both program makers and television viewers. Only the medium of delivery has changed.

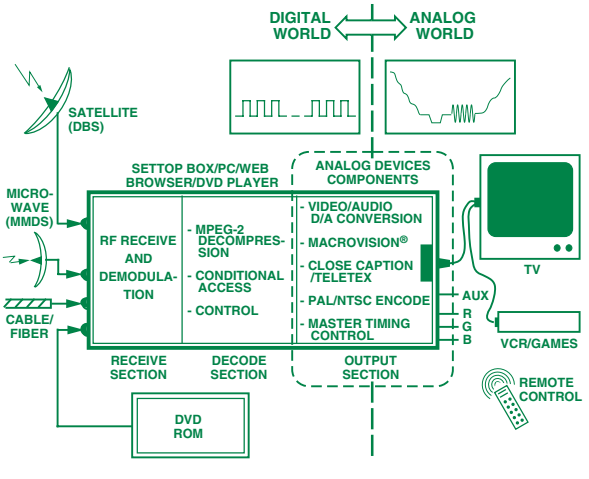


Figure 1. In home digital video architectures, the encoder is key, whatever the source.

*For technical data, visit our Web site, http://www.analog.com. Data is also available in North America around the clock by Analogfax™, 1-800-446-6212; request **1948**; or use the reply card. Circle **5**

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This digital revolution offers a new and very significant feature to viewers. The ability to compress the digital video data means that a great many more viewing channels become available to the consumer using a standard TV set. Up to six channels can now be transmitted in the bandwidth that was previously required for just one. In addition to more channels, the signal quality available in a digital system results in vastly improved displayed pictures.

Figure 1 shows the array of reception options that the home viewer has in the digital video world, including DBS (direct-broadcast satellite), digital cable (coaxial, fiberoptic, etc.) and what is oxymoronically termed wireless cable—in essence, a microwave line-of-sight distribution system, known also as MMDS (multipoint microwave distribution system). The major broadcasting networks have plans to introduce a digital version of the traditional antenna-based transmission system. Besides video broadcasts, the viewer may have local video sources, such as video CD, game console or, indeed, the emerging DVD format.

The received digitally coded TV signal must first be converted back to the traditional NTSC or PAL signal, capable of being understood by the standard TV. The settop box, or integrated receiver decoder (IRD), which interfaces (bridges the gap) between analog and digital worlds, implements these functions:

- Receive and demodulate digital signal (QAM/QPSK receiver)
- Decompress the digital data (MPEG-2 Decoder)
- Convert the digital data into standard TV Signal (NTSC/PAL digital video encoder).

This last function is implemented by the ADV7175/ADV7176. In addition to performing the basic D/A conversion, the device also encodes the component YUV data into the analog composite (CVBS) or S-Video (Y/C) signals for standard analog TVs.

Multimedia PC application: The ADV7175/ADV7176 are also ideally suited for video editing on PCs. *Analog Dialogue* 30-2 (1996) introduced the ADV601 integrated Wavelet Video Codec; combined with the ADV7175/ADV7176 and a video decoder, it provides a complete, low-cost video-capture/editing system on a PC. Like the interface to MPEG encoders, it needs no additional glue logic.

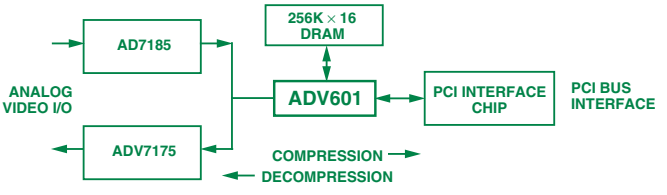
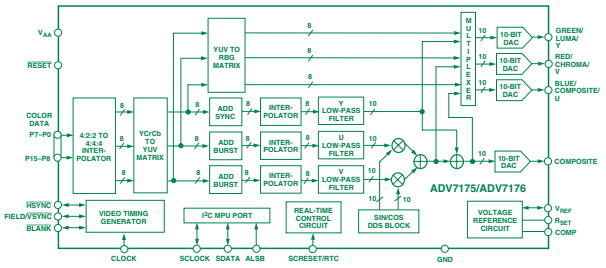


Figure 2. Encoder provides analog output of decompressed video in PC application.

Advanced NTSC/PAL digital encoder: The ADV7175/ADV7176 has been developed in close cooperation with digital video end customers. The resulting parts integrate all the required functionality and features, plus the optimum level of performance at the price levels demanded in the consumer electronics industry.

Beyond four 10-bit DACs, the encoder incorporates our DDS (direct digital synthesis) technology with a 32-bit-wide accumulator to accurately regenerate the color sub-carrier. An extensive input port translates the digital input samples of 4:2:2 YCrCb data into the appropriate luma (Y) and chroma (UV) video signals. A two-wire, I^2C-compatible port allows all functions to be programmed.



The output circuitry enables the part to support the ubiquitous standard composite video formats as well as the increasingly popular performance S-Video (Y/C) video mode. The four outputs mean that the part can simultaneously drive a variety of combinations of CVBS and S-Video. For example:

	Simultaneous composite video and SVHS		SCART format	Professional studio
	Option 1	**Option 2**	**Option 3**	**Option 4**
DAC A	CVBS	Y	CVBS	—
DAC B	CVBS	CVBS	B	U
DAC C	C	C	R	V
DAC D	Y	CVBS	G	Y

For the European market, in which the SCART connector format has become a requirement, the ADV7175/ADV7176 is capable of driving R,G,B & CVBS outputs simultaneously (see Option 3).

The input port enables the device to process industry-standard, CCIR-601 (D1) video data configured in accordance with CCIR-656. The port can be configured for the traditional 16-bit YUV format or the more modern 8-bit format. The associated timing signals of FIELD/VSYNC, HSYNC and BLANK, and the part's ability to operate in a variety of master and slave configurations, means a glueless interface (no additional logic—see Figure 4) between the device and its driving source (e.g., MPEG decoders).

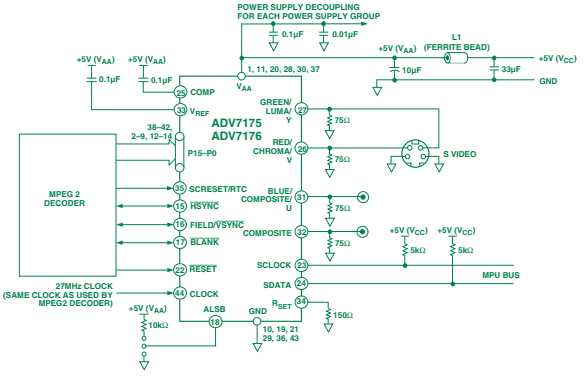


Figure 4. Connection to MPEG decoder.

The ADV7175/ADV7176 is the industry's most comprehensively specified part in terms of functionality, features and performance. Its differential gain (0.8%) and –phase (0.8°) specs are suitable to benefit consumer video applications, and to provide professional studio and broadcasters with a low-cost, highly integrated video encoder. For the benefit of professionals, the part is configurable to output their usual analog YUV format.

Video quality: Performance features also include on-board color enhancements technology, including 2× oversampling, luma low-pass filters, and notch chroma filtering. Oversampling (2 × 13.5 MHz) reduces the requirements on any external low-pass filtering by shifting the out-of-band signals up the spectrum, permitting a lower-order external filter. Figure 5 shows a vectorscope plot of the device output. The proximity of the vertices to the centers of the square boxes, and the linearity of the lines between the vertices, illustrate the device's performance, including the ability to reproduce the required color output values.

Additional features: Also supported are other key functions, programmed via the 2-wire serial (I^2C-compatible) MPU Port.

- *Square Pixel:* in addition to the standard CCIR-601 pixels, square pixel mode is needed to ensure correct aspect ratio when displaying computer-generated images, using a standard TV screen as a computer monitor.

Required sampling frequency	Format	Pixels/line
13.5 MHz	CCIR601 (NTSC/PAL)	720
12.27 MHz	NTSC Square Pixel	640
14.75 MHz	PAL Square Pixel	768

- *Genlock/RTC:* Enables coherent synchronization between two color sub-carrier frequencies of simultaneously displayed video signals (necessary to maintain backward compatibility for simultaneously transmitted traditional analog TV signals)
- *On-board color bar generator:* For system test/diagnostics
- *Programmable luma delay* (for CVBS signal to RF tuner)
- *Closed captioning:* Legal requirement to provide support to display subtitles on television programming
- *VBI (Vertical blanking interval) passthrough:* The VBI consists of transmitted lines with no video information. Not only is it used to transmit teletext data, closed caption data and test/control bits; this portion of the video signal is also being deployed to deliver Internet or Web Page data to the TV viewer
- *Programmable frequency and phase:* Ensures that all terrestrial variants of PAL and NTSC can be configured.

Thermally enhanced packaging: Fitting such functionality into a tiny 44-lead PQFP package demands advanced techniques in both chip and package design. The device is specified, worst case, to drive full video outputs from all four DACs without needing external buffering. Advanced current switching techniques, which minimize dissipation during the display of low brightness scenes, coupled with a patented thermal-coastline lead-frame design within the package, ensure that the complete functionality of the part is made available to the user in all environmental conditions. Additional programming, allowing the selective turning off and on of each of the 4 DACs, offers yet more configuration options to minimize total power consumption.

Though specified to run from 5-V supplies, measured data shows that it will satisfy the video specs with negligible degradation at 3.3 V. The ADV7175/76 is available from stock. An evaluation board can also be ordered. Device prices (10,000) start at $7.59.

The ADV7175 was developed in Limerick, Ireland, by a cross-functional team led by Joe Canning, Colin Prendergast, and John Purcell. A

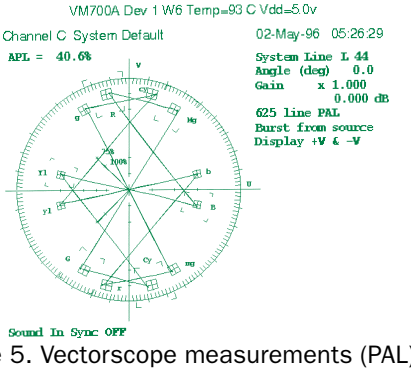


Figure 5. Vectorscope measurements (PAL).

Selecting Mixed-Signal Components for Digital Communication Systems-II

by Dave Robertson

Part I, in Analog Dialogue 30-3, provided an introduction to channel capacity and its dependence on bandwidth and SNR. This installment discusses a variety of modulation schemes, and the demands each places on signal processing components.

Digital Modulation Schemes: The first installment in this series showed how limitations of SNR and bandwidth constrain the bit capacity of a communication system that uses pulse amplitude to convey bit information. As a way to encode digital bits, pulse amplitude is one of many modulation schemes used in digital communications systems today; each has advantages and disadvantages. We define below some of the more common modulation types, highlighting their basic principles, and noting the typical component specifications that impact performance. The textbooks listed on page 12 can provide more complete descriptions of these modulation schemes.

PAM—pulse amplitude modulation: (discussed earlier) encodes the bit values in the amplitude of a stream of pulses sent down the channel. The theoretical bandwidth (in Hz) required is at least 1/2 the symbol rate; practical implementations use more bandwidth than this. PAM is typically a baseband modulation scheme: it produces a signal whose spectral content is centered on dc. The simplest case, where each symbol represents the presence or absence of a single bit, is called pulse-code modulation.

Since the bit value is encoded in the amplitude of the signal, gain and offset of the components in the signal path affect system performance. Higher-order modulation schemes using more than two levels will need correspondingly better amplitude accuracy in the system components. Offset, which can shift the signal from the proper level threshold, creating a biased tendency to misinterpret bits high (or low) in the presence of noise, should be controlled. Bandwidth of the components is also an important consideration. As shown earlier, limited bandwidth produces undesirable intersymbol interference. Filtering may be used to carefully control the bandwidth of a transmitted signal, but signal processing components should not unintentionally limit the bandwidth. Generally, components should have enough bandwidth so that the channel itself is the band-limiting factor, not the signal processing circuitry.

AM—amplitude modulation: closely related to PAM, straight AM represents transmitted data by varying the amplitude of a fixed-frequency carrier, usually a sine wave, of designated frequency, f_C. Conceptually, this can be produced by taking the basic PAM signal, band-limiting it to reduce harmonic content, and multiplying it by a carrier at a fixed frequency, f_C. The result is a double-sideband signal, centered on the carrier frequency, with bandwidth twice that of the bandlimited PAM signal.

As with the PAM case, components in the signal chain must be selected to maintain amplitude integrity within the band centered around the carrier frequency, f_C. In this case, analog components may be evaluated based on their linearity, THD (total harmonic distortion) or SFDR (spurious free dynamic range) performance at f_C. For multi-bit symbols with numerous distinct amplitude levels, noise may be an important consideration in component specification.

FM/FSK—frequency modulation/frequency shift keying: We've shown that amplitude modulation schemes (including PAM) can be very sensitive to voltage noise and distortion. Alternatively, information can be encoded in the *frequency* of the sine wave being sent, so that signal attenuation or other amplitude-based disturbance would not tend to corrupt the recovered data (FM radio's resistance to static and signal degradation compared to AM are well-known analog examples; similar principles apply for digital transmission). In a simple binary case of one-bit-per-symbol, the transmitted signal would shift between frequencies f_0 ("0") and f_1, ("1"), on either side of an average, or carrier, frequency—*frequency shift keying* (FSK). It is important to note that the transmitted signal bandwidth actually spreads over a larger bandwidth than just the span between f_0 and f_1, because the speed of transitioning between the two frequencies generates additional spectral content. To simplify receiver design, it is desirable that the symbol rate be substantially less than the difference between f_0 and f_1; this makes changes in frequency easier to detect.

Frequency modulation significantly reduces the sensitivity to amplitude errors in the signal path. Since all the useful information is held in the frequency domain, many FSK receivers feature a *limiter*, a high-gain circuit designed to convert a variable-amplitude sinusoidal signal to a more nearly constant-amplitude square wave, desensitizing the circuit to component non-linearities and making it easier for subsequent processing circuitry to detect the frequency of the signal (even by counting crossings within a given time interval). Signal bandwidth is at least as important as with AM: intersymbol interference still results from insufficient processing bandwidth. Because a carrier frequency must be processed, the required bandwidth is probably significantly larger than PAM modulation of the same data. These systems are typically more sensitive to timing errors, such as jitter, than to voltage noise.

PM/QPSK—phase modulation/quadrature phase shift keying: phase and frequency are closely related mathematically; in fact, phase is the integral of frequency (e.g., doubling frequency causes phase to accumulate at twice the original rate). In PM, the signal is encoded in the phase of a fixed-frequency carrier signal, f_c. This can be accomplished with a direct digital synthesizer (DDS) that generates a digital sine wave, whose phase is modulated by a control word. A D/A converter restores the sine wave to analog for transmission.

Another example of how a 2-bit phase-modulated symbol may be derived can be seen with two equal sinusoidal components at the same frequency: in-phase (I) and quadrature (Q), 90° apart, each representing digital "1" if non-inverted, "0" if inverted (shifted 180°). When they are added, their sum is a single wave at the same frequency with 4 unique phases, 90° apart (i.e., 45°, 135°, 225°, and 315°), corresponding to the phases of the I and Q waves. Figure 1 is a "unit-circle" or "satellite" plot, graphically representing these combinations. Systems embodying this principle of phase modulation are often referred to as quadrature phase-shift keying (QPSK). As with FM, the relationship between the bandwidth of the transmitted spectrum and the symbol rate is fairly complicated. There are several variations of phase modulation, including DQPSK (differential QPSK). These types of modulation schemes are popular in difficult environments such as cellular telephony,

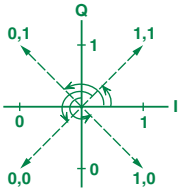


Figure 1. 2-bit QPSK phases.

because the phase information can be maintained in the presence of noise and the distortion introduced by power amplifiers.

As with FSK, components for PSK systems are typically selected based on bandwidth and other frequency domain specifications. Limiters may be used to eliminate amplitude noise. Timing errors, including jitter, effectively become "phase noise," making it more difficult to properly interpret the received signal. Modulator/demodulator units may be implemented in a quadrature arrangement, where the I and Q components are separated and processed separately through part of the signal chain. Here amplitude- and phase match between the I and Q paths are important specifications, since any mismatches map to an effective phase error.

QAM—Quadrature Amplitude Modulation: Returning to Figure 1, the representation of the four different phases of the carrier in a QPSK system, note that each of the phases also has an amplitude that is the vector sum of the I and Q amplitudes; since the amplitudes are equal, the amplitudes of the vector sums are equal. More bits per symbol could be transmitted if, instead of just two levels for I and Q, they were further quantized; then, by adding the differing amounts of sine (I axis) and cosine (Q axis) together, the combination in vector sums would modulate both amplitude and phase. Figure 2a shows the use of 2-bit quantization of both I and Q to realize 16 unique states of the carrier in each symbol, allowing transmission of 4 bits per symbol. This modulation could be produced by varying the phase and amplitude of the generated carrier directly using, for example, direct digital synthesis. More commonly, amplitude-modulated I and Q (sine and cosine) versions of the carrier are combined.

Hence the term *quadrature amplitude modulation* (QAM): the two quadrature versions of the carrier are separately amplitude modulated, then combined to form the amplitude- and phase-modulated resultant. The plot in Figure 2a, showing the various possible combinations of I and Q, is referred to as a "constellation." Note that very large constellations can, in concept, be used to represent many bits per symbol, with a required bandwidth similar to simple QPSK of the same symbol rate. The points of the constellation represent the transmitted signal and the expected value of the received signal; but noise or distortion will displace the received signal from its ideal position; it can be misinterpreted as a different constellation point if the error is large.

Figures 2a and 2b compare the 16-point constellation (2 bits I and Q) to a 64-point constellation (3 bits I and Q). At similar transmitted power levels the constellation points for the 6-bit case are twice as close together, therefore the "error threshold" is 1/2 as large and, for a given bit error rate, a 6-dB (approximately) better signal-to-noise ratio is required. The table shows typical SNR requirements for various sizes of QAM constellations to realize a 10^{-7} bit error rate. Note that binary I & Q information can be encoded [e.g., Gray code] so that points representing adjacent or nearby transmitted signal levels have similar bit patterns. In this way, misinterpreting a constellation point for one of its neighbors would corrupt only 1 or 2 bits of a multi-bit symbol.

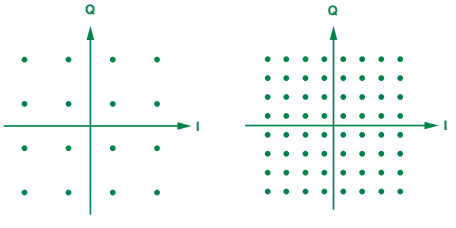


Figure 2. QAM constellations. a) 4 bits: 2-bit I and 2-bit Q. b) 6 bits: 3-bit I and 3-bit Q.

Bits/symbol (I,Q)	QAM constellation size	Required SNR
2 (1,1)	4 (QPSK)	14.5 dB
3 (1,2)	8	19.3 dB
4 (2,2)	16	21.5 dB
5 (2,3)	32	24.5 dB
6 (3,3)	64	27.7 dB
7 (3,4)	128	30.6 dB
8 (4,4)	256	33.8 dB
10 (5,5)	1024	39.8 dB
12 (6,6)	4096	45.8 dB
15 (7,8)	32768	54.8 dB

Here are some of the important specifications for components selected for QAM signal processing. *Bandwidth* should be sufficient to handle the carrier frequency, plus enough frequencies within the band to avoid introducing intersymbol interference. *Total harmonic distortion* (THD) at the carrier frequency is an important consideration, since distortion will tend to corrupt the amplitude information in the carrier. *Jitter* should be minimized to ensure that the phase information can be properly recovered. *Matching* of amplitude and phase between the I and Q processing blocks is important. Finally, *noise* (quantization and thermal) can be an important consideration, particularly for high-order constellations. Wherever practical, components should be selected to ensure that the channel itself is the noise-limiting part of the system, not the components of the signal processing system. QAM can be used to transmit many bits per symbol, but the trade-off is increased sensitivity to non-idealities in the communications channel and the signal processing components.

This provides a quick review of the basic modulation schemes. The many variations, combinations and enhancements of these approaches seek to deal with the characteristics of particular applications and the shortcomings of the various transmission techniques. They offer trade-offs between spectral efficiency, robustness, and implementation cost.

The next part of this series will explore multiplexing schemes and the variety of dynamic range requirements encountered in digital communications systems. A

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Voltage Regulators for Power Management

by Jürgen Kühnel

Portable electronics is becoming more popular as laptop computers and telephones become smaller in size and lighter in weight. This has intensified the focus of system designers on reducing the size and the weight of the electronics in general, and power supply circuits in particular. Such considerations as board space, system cost, number of components, availability, and battery life have become increasingly important. Indeed, battery life has become a key selling feature of portable equipment, as users can expect today's system to operate for a much longer time than one purchased just two years ago.

Among the many applied strategies to achieve cost savings, improved efficiency and the reduction of size are the most important. The use of the latest low-dropout regulators (LDO) or fast switching regulators has reduced the loss of energy in these power supplies, leaving more energy for the rest of the system operation. New battery technologies have also served the same purpose, either reducing the size without reducing capacity, or improving capacity while retaining the same size (and weight). Standby (or sleep) modes make sense, especially when power conversion occurs locally, close to the respective loads. The system can thus switch off unused sections—such as a hard drive in a laptop computer, or the transmitter in a phone.

The newer regulators make it possible for the designer to reduce the size and overall cost of the total system solution, because they can also use smaller and less expensive external components, such as capacitors and inductors.

Simple linear voltage regulators have been around for a long time; but although they are low in cost, their dropout voltage—the minimum voltage drop across the pass transistor—is relatively high, usually between 1.5 and 3 V. The development of low-dropout regulators (LDOs), with dropout voltages as low as 0.1 V to 0.4 V per 100 mA of load current—reducing dissipation in the regulator by some 90%—was a major improvement. Besides the lower dissipation than is the case for the simple regulators mentioned above, either a lower voltage battery can be used or the battery can discharge down to a lower voltage before it needs to be replaced or recharged. This translates into longer operating time.

Low-dropout voltage regulators from Analog Devices include:

- the general-purpose ADM66x family and the ADP3367*, with dropout voltage levels from 1 V down to 100 mV per 100 mA.
- a new generation of high-performance, ±0.5%-accuracy *anyCAP*™ LDO regulators, the ADP3300, ADP3301, and ADP3303 for 50, 100, and 250 mA full-scale output, with dropout levels of 100 or 200 mV per 100 mA.
- a dual 100-mA version of the ADP3301, the ADP3302, features the same ±0.5% accuracy and low 120-mV dropout levels.

Traditional LDOs need a bulky, expensive 10-µF load capacitor with carefully chosen equivalent series resistance (ESR); the ADP330x series can operate with a wide range of capacitor types and values—a typical example might be a 0.47 µF, low cost multilayer ceramic capacitor. This significant technology is patented and has been trade-marked "anyCAP™".

LDOs are more efficient than conventional linear regulators and extend a battery's useful operating voltage, but their voltage drop wastes precious power [$W = (V_{IN} - V_{OUT}) \times I_L$]. All linear regulators require a higher input voltage than output voltage; they can only regulate down to the desired value, never boost up to it. So for higher efficiency, and the flexibility to have the output voltage exceed the input voltage or go negative, designers must turn to a switched-mode or a switched-capacitor regulator or converter.

By eliminating the dissipation of the pass transistor, switch-mode regulator circuits [see sidebar] can have efficiencies of 90% and more. Thus, more battery energy goes to the powered equipment, resulting in increased operating time. In obtaining high efficiency, however, switch-mode regulators also pose some challenges. For example, the need for a magnetic component increases the power supply's overall size and weight, both of which may be critical in portable equipment design; it also adds to the system cost.

To minimize these problems, switching frequencies are being pushed higher—up to 1 MHz in some cases—to reduce the size of inductors and capacitors. However, switching regulators have another issue: Operating in either pulse-frequency modulation (PFM) or pulsewidth modulation (PWM)[1] mode, input and output ripple and electrical noise (electromagnetic interference, or EMI) are generated when the current is switched.[2] Thus, depending on the application, switch-mode regulators may require filters to smooth the output ripple and/or shielding to suppress EMI. Nevertheless, the higher efficiency of switched-mode regulators has made them popular in applications such as laptop computers.

One of the *switching regulators* being introduced by Analog Devices is the ADP3000 (see sidebar).* It can operate in boost, buck and inverter modes. In *boost* mode, it accepts input voltages from 2 V to 12 V, and in the *buck* mode, inputs up to 30 V. Fixed voltages of 3.3 V, 5 V and 12 V are offered, as is an adjustable output.

Several key features make the device well suited for portable battery-powered applications. For instance, it draws only 500 µA in the quiescent, or standby mode. The 400-kHz switching frequency means that only a small external inductor is needed. In most cases, the smallest-size inductor available (2.2 µH up to 15 µH for 1 A peak current) will suffice. Other key features are the low output voltage ripple[3]—less than 40 mV p-p at 3.3-V output—adjustable current limit, and an auxiliary amplifier that can serve as either a low-battery detector, linear regulator, voltage lockout or error amplifier. The example below will show how these features are used in an actual application.

Switched-capacitor voltage converters are another technique to avoid the losses associated with LDOs. An example is the recently introduced ADP3604* switched-capacitor voltage inverter with regulated output. This device delivers a regulated voltage with minimum voltage loss, very few external components, and no

*For technical data, use our Web site, http://www.analog.com, phone our Analogfax™ number, or use the reply card; for ADM66x and ADP3367, **circle 6**; for ADP330x, **circle 7**, for ADP3000, **circle 37**, for ADP3604 **circle 38**

[1]PFM uses constant-*on*-time pulses but changes their frequency, depending on load and input voltage. This generates unpredictable interference with other system frequencies, such as system clocks, IF in telephones, etc. The frequency, starting at a few hundred Hz, will cross through the complete audio range; the problems it creates are another reason PFM technology is not well accepted in anything that contains some sort of audio. PWM uses a fixed frequency but alters the width of the pulses; its noise is therefore easier to filter.

[2]Switching pulses contain spikes with 20-ns to 40-ns rise times; these generate most of the EMI problems.

inductor or transformer. With a 240-kHz internal oscillator producing a 120-kHz switching frequency, the ADP3604 uses significantly smaller and cheaper capacitors than earlier designs such as the ADM660 and ADM8660. It accepts an input voltage between +4.5 V and +6.0 V and produces an output voltage of –3 V, with ±3% accuracy and up to 120 mA of output current.

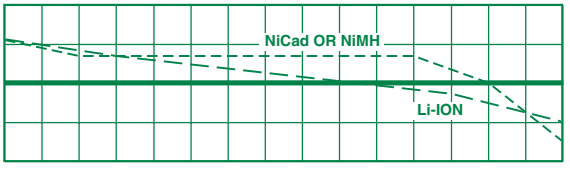


Figure 1 Typical battery discharge curves. The horizontal line represents the desired 3-V constant output.

As mentioned above, battery technology has made great progress, too. Though not much used in the past, the lithium-ion (Li-ion) types become the battery of choice for many recent applications, for good reasons: They have the best energy density (ratio of charge capacity to weight), and they have long standby times, due to a very low self-discharge current. But they do have a behavior that makes them hard to use without sophisticated electronics. Their output voltage drops constantly over the time of discharge. Unlike Ni-Cd or NiMH cells, which have a lengthy plateau and then a rather sharp drop at the end of capacity (Figure 1), a Li-ion cell starts at a voltage of 4.1 V to 4.2 V (depending on the chemistry, and the specific manufacturer); then, while it is discharged, the voltage drops almost linearly all the way down to about 2.5 V. Beyond that point, since further discharge can damage the battery, it needs to be recharged.

The circuit shown in Figure 2 was designed to generate two constant 3-V outputs of up to 100 mA each from a single Li-ion cell. The output is maintained within ±1% over a range of input from 4.2 to 2.7 V, load from 0 to 100 mA per output, and operating temperature from –40 to +85°C. The circuit has auto-shutoff to protect the battery when the input voltage has dropped to 2.5 V.

A constant +3-V output can be generated from a varying input voltage, with either an LDO or a *buck*-regulator (when the input is always larger than the +3-V output) or with a *boost*-regulator, when input is always smaller than +3 V. For the example of developing +3-V output from a single Li-ion cell over an extended life, it is necessary to provide boost when the input is less than 3.1 V, and stepdown above that voltage. There are several ways to do this. For example, an ADP1147-type stepdown switching regulator could be used in the flyback mode. The disadvantage is the ripple on both the input and the output. Or the ADP3000 could be used in a single-ended primary inductance converter circuit (SEPIC), an application shown on the data sheet, using two inductors; its weakness is rather large ripple. The ADP3000 circuit of Figure 2, with an ADP3302 dual-output LDO, is optimized to operate with smallest shielded 6.8-µH inductor to save space and money. Even smaller and cheaper are open inductors—rod types—which can be used when the environment of the power circuit is not sensitive to EMI.

Here is how the circuit works: Initially, the battery is fully charged. The input voltage is well above 3 V, and the switching regulator ADP3000 is in idle mode because the voltage at Fb (ADP3000, pin 8) is above the reference voltage (1.245 V). The LDOs (ADP3302) regulate the output voltage at 3 V. The load current (up to 2 × 100 mA) flows steadily through the inductor (resistance of 0.12 Ω), and the Schottky diode (D1) with < 0.2 V forward voltage, for a total voltage drop of about 0.23 V.

As the battery voltage decreases with time, the voltage at Fb decreases proportionally. As the input drops below about 3.7 V, the voltage at Fb goes below the 1.245-V reference voltage (voltage divider R9–R10). The internal comparator changes state, the oscillator of the ADP3000 starts; the boost converter—built up with the inductor and the diode—begins to transfer energy into capacitor C3 to keep the voltage at Fb at around 1.245 V. The lower the battery voltage drops, the more energy has to be transferred, resulting in an increasing switching frequency, that reaches well above 100 kHz just before shutdown (at 2.5 V), given a 200-mA full load[4].

The SET input of the ADP3000 (pin 7) continously monitors the input voltage via the R1-R2 divider. When it falls below 2.53 V (between 2.74 V and 2.53 V, depending on the reference inside the ADP3000), Ao (Pin 6) will go to a logic LOW and shut down the ADP3302 LDO regulator by pulling SD1 & SD2 (Pins 6 & 7) to ground. At the same time, the transistor is turned on (voltage divider R5-R6) to pull Fb up and ensure that the oscillator is shut down. The remaining load current at the battery is just 500 µA from the ADP3000, plus an optional micro-LED connected to Ao as a battery depletion alarm to the user (dotted).

The 33-nF capacitor (C2) is used to filter feedthrough from the supply voltage into the sensitive feedback point, Fb. The 120-Ω resistor (R4), connected to I_{LIM}, limits the switch current to lower the requirements for the inductor's current rating, at the same time reducing the output ripple and required capacitance.

The ADP3000 was designed at Analog Devices, Santa Clara, California, by James Ashe. A

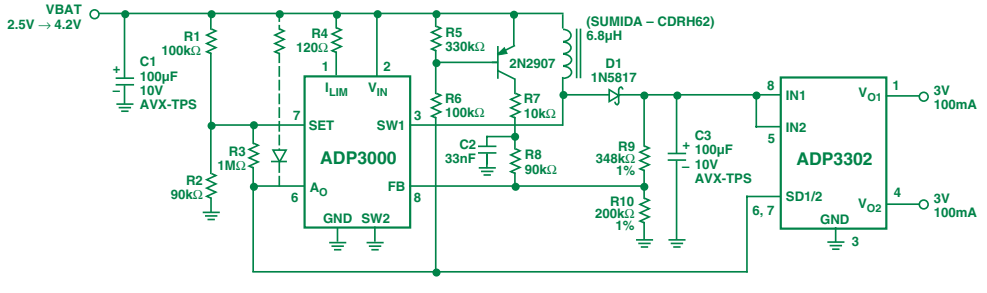


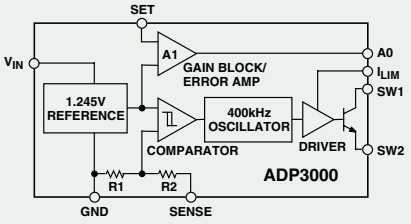
Figure 2. A regulator to maintain two 3 V outputs using a Li-ion battery.

[3]Output ripple is a function of switch-peak-current × ESR (equivalent series resistance of the output capacitor). ADP3000 reduces ripple by limiting the peak current [I_{LIM}] and using capacitors that have low ESR, such as Sony OS-COM (1.5 mΩ)]. The tantalum capacitors recommended for standard switching converters (which also lack the current-limiting feature) have ESR of about 100 mΩ.

[4]The oscillator runs at a constant 400 kHz, but a gating circuit, which lets the required number of pulses through, is responsible for the resulting frequency seen at the output.

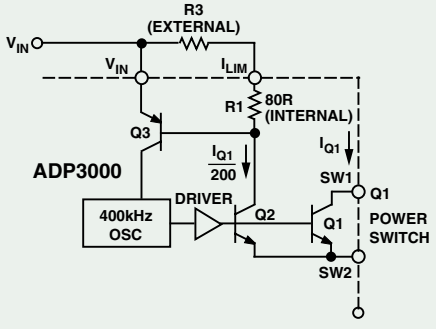
The ADP3000 is a versatile step-up/step-down switching regulator. It operates from 2 V to 12 V in the step-up mode, and up to 30 V in the step-down mode. ADP3000 has a low 500-µA operating current (with the oscillator shut off) and operates with a gated-oscillator (up to 400 kHz) to make it possible to use very small inductors and capacitors.

The functional block diagram shows the main sections of the device: The 1.245-V reference is connected to one input of the comparator; the other comparator input is from the feedback-sense terminal. The output of the comparator gates, the oscillator on/off. Hysteresis stabilizes the comparator's switching.



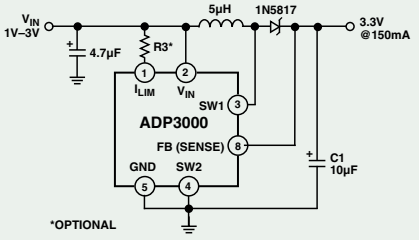
When the voltage at the FB pin drops below the reference voltage, the oscillator is turned on. This oscillator is set to a 2:1 mark/space ratio, with 1.7 µs ON and 0.8 µs OFF—ideal for applications that need a factor of about 2 between the input voltage and the output voltage, such as +3 V to +5 V or +5 V to +12 V. All other conversion factors can be achieved, too, like +5 V to +3.3 V. The oscillator is turned OFF when the voltage Fb is higher than the reference. The fixed-voltage versions of the ADP3000 contain a precision voltage divider, as shown, so that the Fb pin can be directly connected to the output voltage; the adjustable version (used in the example of Figure 2) requires an external voltage divider to set the correct output voltage.

Another control that can shut off the output from the oscillator is, the current limit, I_{LIM}. In this circuit, without an external resistor, the current limit is set by an internal 80-Ω resistor to 1.5-A peak current in the switch. The current in Q2 is 0.5% of the current in Q1, the power switch. When the voltage at the base of Q3 crosses 0.6 V, Q3 opens and shuts off the oscillator. Resistance added externally (R3) reduces the value of I_{PEAK}. R3, in conjunction with the internal 80-Ω resistor, limits the current in the switch: $R_3 = (120\ V/I_{PEAK}\ A) - 80\ \Omega$. If a small inductor is used, it is necessary to limit the current to prevent saturation of the core.



BOOST MODE

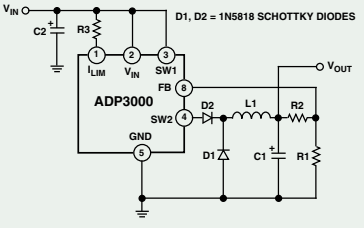
In the application shown in Figure 2, the ADP3000 is used in boost (step-up) mode, i.e., it accepts voltages between 2 V and 12 V and generates an output voltage greater (more positive) than this input voltage. The next figure shows the very basic configuration for a fixed-voltage ADP3000, i.e., a 3.3-V, 5.0-V or 12-V version.



As shown, the inductor is connected between the positive input voltage and the collector of the switch. Note that for an output of 3.3 V and 150 mA only 5 µH inductance is needed (currently, the smallest-physical-size inductor from Sumida is type CDH53). This is made possible by the high operating frequency of the ADP3000. The boost function is achieved by periodically connecting the inductor to ground (switch is ON), then disconnecting it again. When the switch is ON, current starts flowing from V_{IN} to ground via the inductor. Before current through the transistor can build up substantially, the inductor is disconnected by switching the transistor OFF. Since inductor current seeks to continue flowing, it flows through the Schottky (for low dissipation) diode and gets rid of the magnetic field's stored energy by building up an increment of charge on the capacitor during the second half of each cycle. The voltage on the capacitor will be *higher* than the input voltage. Fb monitors this output voltage and, as described above, controls the oscillator/switching, skipping cycles when the output is too high.

ADP3000 IN BUCK-MODE

In the buck or step-down mode the ADP3000 can accept input voltages up to 30 V, making it attractive for a wide variety of automotive and industrial applications. Basically, the same external components are used, but the inductor is connected between the emitter of the switch and the output capacitor:



When switch is ON, current starts flowing through the switch transistor via the diode into the inductor. When set to OFF, the transistor current stops flowing, but the inductor current keeps flowing, thus bringing the pin SW2 below ground. (As this point can only accept a maximum of –0.5 V, diode D1 has to be a Schottky type.) The capacitor is charged, but this time with a voltage lower than V_{IN}. The ADP3000 used here is an adjustable type; the resistors R1 and R2 are the external voltage divider; Fb is connected at the divider point, and the nominal value of controlled output voltage is $(1 + R_2/R_1) \times 1.245$ V.

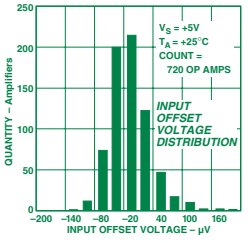
A second diode, D2, not shown in the boost regulator, is needed for output voltage above 6.2 V, the maximum the switch can tolerate. D2 simply isolates high voltages from the switch.

As shown, only a few small external components are needed to use the ADP3000. Due to the high operating frequency, only very small inductors and capacitors are used, saving significant space and some cost. ADP3000 is available in an 8-lead plastic DIP or SOIC package. Pricing starts at $2.14 in 1000s.

Three New Op Amp Families

Single/Dual Rail-Rail

Single-supply OP162/OP262
325 μV V_{OS}, 15-MHz 650 μA I_{SY}



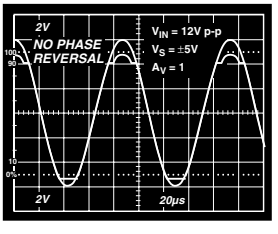
The single OP162 and dual OP262 operational amplifiers combine low offset (325 μV max, 45 μV typical), wide bandwidth (15 MHz), and low power (650 μA max per amplifier—OP262 @ +25°C, +3-V supply). They will operate with single supplies from +2.7 to +12 V and are completely specified for operation at +3 V, +5 V, and ±5 V. A quad version, OP462, is also available.

Their low offset is accompanied by low drift and noise (1 μV/°C, 9.5 nV/√Hz at 1 kHz, (0.5 V p-p from 0.1–10 Hz). Bias current is 600 nA max (360 typical), and current noise density at 1 kHz is 0.4 pA/√Hz. The amplifiers are unity-gain stable, can slew at 10 V/μs and settle to 0.1% of a 2-V step in <0.6 μs. They can be overdriven without suffering phase inversion.

Their outputs can swing rail-to-rail, i.e., to within 0.05 V max of either supply terminal with 250 μA load current, and to within 0.15 V max at 5 mA. Maximum output current is typically ±30 mA, and short-circuit current is ±80 mA.

Operating temperature range is –40 to +125°C. The OP162G and OP262G are available in 8-pin plastic DIP and SOIC; the OP162H and OP262H are available in 8-pin TSSOPs. Respective prices (1000s) are $1.52, $2.19, $1.63, & $2.27.

Faxcode* 1951 or Circle 8 A

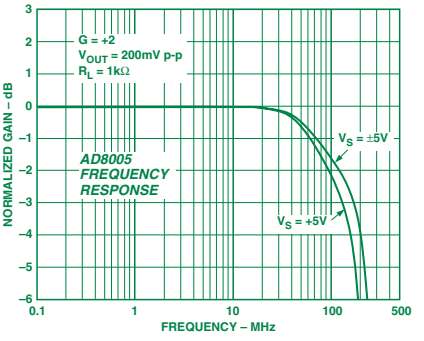


Low-Power, High-Speed Amplifier

AD8005 draws only 400 μA of supply current, has 270-MHz bandwidth, 280 V/μs slew rate, 28-ns settling

The AD8005 is a current-feedback operational amplifier combining low power, high speed and fast settling—with good video specifications, and low distortion. It is especially useful as a power-conserving high-speed amplifier for signal conditioning in the signal chain, furnishing moderate drive current (10 mA). Typical applications include battery-powered portable equipment; loop-powered equipment—such as telecom line cards; and high-component-density systems requiring minimum dissipation.

It is specified for operation on ±5-volt dual and +5-volt single supplies, drawing typically 400 μA of quiescent current (560 μA worst case, over temperature—–40 to +85°C—with ±5-V supplies). It has a bandwidth of 270 MHz at gain of +1, and 170 MHz at +2, with 280 V/μs slew rate and 28-ns settling time to 0.1% (2-V step). For



video applications, its differential gain and phase errors are 0.11% and 0.4°, and its gain is flat within 0.1 dB to 30 MHz.

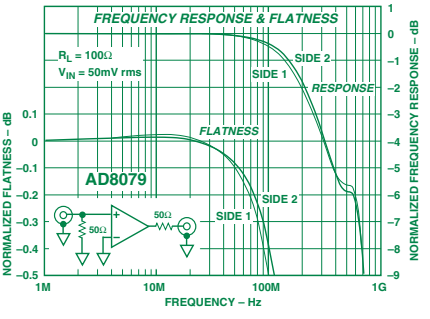
Distortion is –63 dBc at 1 MHz and –50 dBc at 10 MHz; and noise at 10 MHz is only 4 nV/√Hz. The AD8005 is currently available in DIP and SO-8—and will shortly be available in 5-pin SOT23. Price in 1000s is $1.45. **Faxcode* 2053 or Circle 9** A

Gain-of-2 Buffer Amplifier: 260-MHz BW

Dual AD8079 is available with gains +2.0 and +2.2 for video buffering: 50-MHz flatness; 0.01% ΔG, 0.02° ΔΦ

The AD8079 is a dual fixed-gain buffer amplifier with principal applications in video systems—for example, differential and single-ended line driving. It is ideal for driving and unloading video crosspoint switches, such as the 16 × 16 AD8116. It is available in two versions (A, B) with gains of +2.0, +2.2. The internal gain-setting resistors and optimized pinout effectively isolate the inverting input from parasitic capacitance, resulting in excellent gain flatness. The B-version's +2.2 gain is useful in compensating for gain losses elsewhere in a system.

It has a –3-dB bandwidth of 260 MHz, with 0.1-dB flatness to 50 MHz; excellent differential gain and phase performance (0.01%, 0.02°); low power drain (50 mW, or 5 mA, per amplifier—5.75 mA max); 0.1% gain matching and low crosstalk (–70 dB at 5 MHz); and its high output



(70 mA) can drive up to 4 video loads per amplifier. Its slew rate and settling time to 0.1% are 750 V/μs and 40 ns, respectively, for a 2-V output step. Distortion is low, at –65 dBc THD for a 5 MHz signal.

Using ±5-volt supplies, it operates from –40 to +85°C and is available in a small 8-lead plastic SOIC package. Both versions are priced at $3.50 in 1000s.

Faxcode* 2072 or Circle 10 A

*For immediate data, visit our **WorldWide Web** site: **http://www.analog.com.** In North America, call ADI's 24-hour AnalogFax™ line, **1 (800) 446-6212** and use **Faxcode.**

A/D and D/A Converters

Ultrafast & Fast 14-bit A/D Converters

3-MSPS AD9243 works on +5 V supply, uses 110 mW
330-kSPS serial-output AD7851 uses +5 V, 60 mW

The AD9243 and AD7851 are two of the fastest 14-bit monolithic A/D converters available today. They are smaller, less costly, and run much cooler than hybrid devices of comparable speed and resolution.

With its 3-MSPS sampling rate and 40-MHz full-power signal bandwidth, the **AD9243** creates a new IC speed class, especially useful in communications and imaging, but of interest in many other fields. Its low dissipation, single 5-V supply, differential inputs, and internal reference, as well as its low price and small package, make possible new applications, as well as providing an ideal upgrade for 12-bit devices.

Besides its 333-ksps sampling rate, 20-MHz full-power signal bandwidth, and serial interface, the **AD7851** has a number of useful features. For example, its already low maximum dissipation of <90 mW can be further reduced to 52.5 μW max in sleep mode; with the external clock on, dissipation in that mode is increased to only 105 µW. The device contains self- and system-calibration options to ensure accurate operation over time and temperature. It powers up with a set of default conditions, and can be operated as a read-only ADC.

Both devices are available for –40 to +85°C operation. The AD7851 has a choice of 24-pin DIP and SOIC, as well as SSOP, packages. **Circle 11** A

	AD9243	AD7851A	AD7851K
Throughput (MSPS)	3.0	0.333	0.285
SNR, dB min*	77	77	78
SINAD, dB min*	76	77	78
SFDR, dB*	91 typ	87 max	87 max
SFDR, dB, A_{IN} @ Nyquist	84 typ	84 max	84 max
THD, dB max*	–80	–86	–86
I_{DD}, mA max (5 V ± 5%)	29	17	17
T_{MIN}/T_{MAX} (°C)	–40/+85	–40/+85	–40/+85
Smallest Package	MQFP-44	SSOP-24	SSOP-24
Faxcode	2036	1873	1873
Price (1000s)	$49	$12.50	$14.75

*A_{IN}: AD9243, 500 kHz; AD7851, 10 kHz

60-MSPS Dual ADC

8-bit AD9059 works on +5 V, TTL/CMOS +3 V or +5-V logic

The AD9059 has two 8-bit sampling A/D converters on a single monolithic chip. Powered from a single 5-V supply, it is a complete solution, including two track-holds and an internal +2.5-V reference. It provides excellent dynamic performance for conversion rates ≤ 60 MHz, with low dissipation (400 mW), wide analog band-width (120 MHz), and 44.5-dB typical SINAD (7.2 ENOB) with 10.3-MHz input. It will operate with +5- or +3-V logic (a separate supply pin powers the digital outputs).

Besides any multi-ADC application, the AD9059 is well-suited to I&Q digital communications (QAM demodulation) in wireless receivers and cable modems. It operates over the full –40 to +85°C temperature range and is housed in a tiny 28-lead SSOP package. Its price (1000s) is $11.88, and $195 for an evaluation board.

Faxcode* 1937 or Circle 13 A

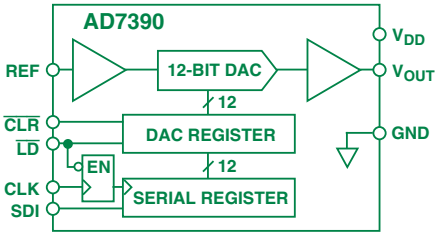
Low-Power DACs need only 100 µA

12/10-bit AD7390/7391 are specified for +3 V & +5 V
Serial input, 1.1-mm-high TSSOP-8 package,

The AD7390 and AD7391 are pin-compatible 12- and 10-bit multiplying D/A converters available in the ultra-thin TSSOP-8 package (just 1.1 mm high). Power consumption is 100 µA max with 3- or 5-volt supply (165 µW typical at 3 V), and output is rail-to-rail. Pin compatibility means that the user can trade off resolution and cost without changing the physical layout. The external reference can be any value from 0 to V_{DD}.

Typical applications are in setting dc voltage set points in digitally controlled calibration and adjustment, for communications, portable instruments, process control, and automotive applications. The TSSOP-8 package is ideal for use in PCMCIA cards.

A double-buffered serial-data interface offers high speed, 3-wire, SPI, and microcontroller-compatible inputs using data-in, clock, and load-strobe pins. In addition, a $\overline{\text{CLR}}$ input sets the output to zero scale at power-on or on user demand.



The AD7390 and AD7391 are specified over the –40 to +85/125°C range, and they are available in plastic DIP and SO-8, as well as TSSOP-8 packages. Prices in 1000s start at $2.80 (10 bits, PDIP & SOIC).

Faxcode* 1957 or Circle 14 A

14-Bit Quad DAC

AD7836's DACs can be individually referenced

The AD7836 contains four 14-bit DACs with ±10-V output (suitable for automatic test equipment), with separate plus and minus reference inputs for each DAC. An override register permits the device to output a user-defined level at any time without affecting the contents of the DAC registers. The ground reference terminal for each DAC is available for applying an external offset voltage. The DACs are 14-bit monotonic over temperature (–40 to +85°C), with 12-bit integral linearity.

Typical applications are wherever multiple DACs with high resolution are needed. Examples include level-setting for pin electronics in ATE, and industrial process control and instrumentation. The AD7836AS is housed in a 44-pin PQFP and requires ±15-V supplies and a 5-V logic supply. Price in 1000s is $22.35.

Faxcode* 2030 or Circle 12 A

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DSPs and Mixed-Signal Processors

Plug-and-Play Audio

AD1815/16 Controllers

Support popular applications

The AD1815 SoundComm™ and AD1816 SoundPort™ Controllers are single-chip ISA Plug-and-Play audio subsystems for adding 16-bit stereo support to personal computers. They provide an integrated solution for Windows 95, Windows NT, OS/2, and DOS-based systems, delivering CD-quality fidelity and 5 channels of digital mixing. The AD1815 includes V.34-class modem I/O capabilities for the cost of a SoundBlaster®-only game audio IC. The AD1816's 3-D Phat stereo enhancement circuitry expands the sound field of typical PC speakers, for increased user immersion.

They add audio capabilities to both motherboards and add-in cards. The AD1815's V.34-capable modem front end (ADC & DAC) can be used for host-based telephony functions, e.g., fax, modem, and speakerphones. The AD1816 can decode other devices for use in multi-function add-in cards.

Features include software and hardware volume controls, an MPC level-2/3 mixer, an integrated FM compatible music synthesizer—plus an MPU-401-compatible MIDI port, an integrated enhanced digital game port, two I^2S digital audio serial port inputs, and a bidirectional DSP serial port; they support dual type F FIFO DMA.

Running on a 33-MHz clock, they have full-duplex capture and playback operation at different sample rates, can support up to six different sample rates simultaneously, and provide programmable sample rates from 4 kHz to 55.2 kHz, with 1-Hz resolution. They employ continuous-time oversampling for low-latency mixing, sample-rate conversion, and signal-stream synchronization of multiple audio, communications, and video signals having disparate sample rates.

The AD1815 and AD1816 have built-in 24-mA bus drivers. They operate from 5-volt supplies. A power-down mode is available. They are housed in 100-pin PQFP and TQFP packages. Prices of the AD1815JS/AD1816JS are $17.50/$18.50 (1000s). **Circle 15** A

16-Bit Fixed-Point DSPs Trim Cost, Space

ADSP-2185 and ADSP-2186 have 32/16K on-chip RAM

3.3-volt versions available for these and ADSP-2181

Two new members of the ADSP-218x line of embedded-SRAM fixed-point DSPs (*Analog Dialogue* 28-3, p. 12) add ultra-low cost and small size to the family's long list of key benefits for designers. The new additions are the ADSP-2185, with 32 K words of built-in SRAM, and the ADSP-2186, with 16 K words of SRAM.

Squeezed into compact 100-pin thin quad flatpacks (TQFP), these new members conserve circuit board area, making them suitable for applications in tight spaces or requiring multiple processors. Typical applications that can benefit from the smaller processors are modem functions for Internet service providers and voice compression at central-office switch networks.

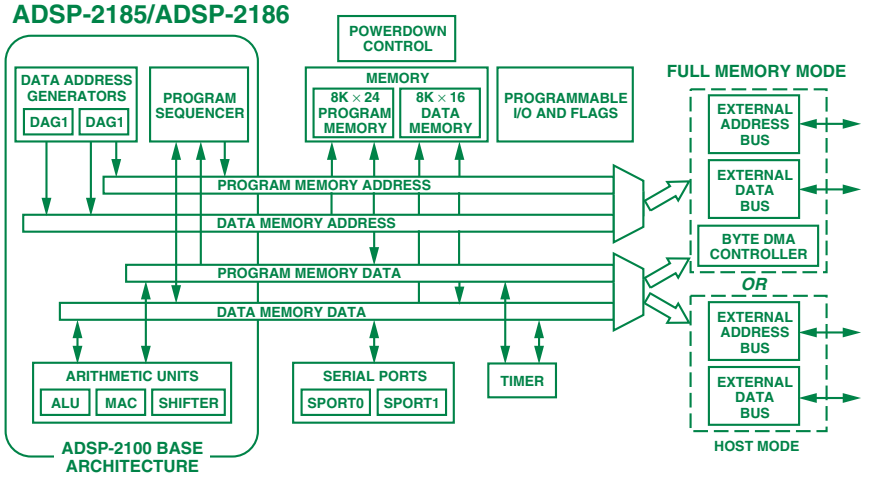
Besides their small size, they are available in a choice of 5-volt or 3.3-volt "L" (for low-power) versions (an ADSP-2181 version is also available for 3.3 V—ADSP-2183). The ADSP-2185 and ADSP-2186 also sport considerably lower prices: $17.10 and $9.90 in very large quantity.

Like other ADSP-218x products, these devices have a great many input/output (I/O) and direct memory access (DMA) features that speed data throughput without burdening the processing core. The designer has choices: a 16-bit internal DMA port that gives a host processor access to the DSP's on-chip memory; a byte DMA port that can access instructions and data stored in low-cost external EPROMs; and a pair of on-chip serial ports that connect directly to high-speed telecommunications networks.

To fit into smaller packages, yet still offer the full range of memory access features, both chips multiplex some serial-port, programmable-flag, interrupt, and external bus functions.

The new DSPs are pin-compatible; that is, designers can interchange them to fit the price/performance goals of a particular end use. What's more, both can execute code written for ADI's ADSP-2100 fixed-point DSP family, the industry's largest family of code-compatible DSPs. For data on ADSP-2181/2183, **Circle 16**. For data on ADSP-2185/2186, **Circle 17**. A

Processor	Supply Voltage	On-Chip RAM PM	DM	Package
ADSP-2181	5	16 K	16 K	128-PQFP, TQFP
ADSP-2183	3.3	16 K	16 K	128-PQFP, TQFP
ADSP-2185	5	16 K	16 K	100-TQFP
ADSP-2185L	3.3	16 K	16 K	100-TQFP
ADSP-2186	5	8 K	8 K	100-TQFP
ADSP-2186L	3.3	8 K	8 K	100-TQFP



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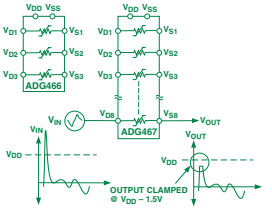
Mixed Bag: Channel Protectors, Temperature, Sw-Cap Inverter

Multiple Channel Protectors

Three-channel ADG466, 8-channel ADG467 Provide overvoltage and fault protection

The ADG466 and ADG467 are monolithic ICs containing 3- and 8-channel protectors. When connected in series with the signal path, they will protect sensitive components from steady-state or transient overvoltage and fault conditions of up to ±40 V.

Each channel protector consists of three MOSFETs in series—an *n*-channel, a *p*-channel, and an *n*-channel (separated by a dielectric trench to prevent latchup). In normal operation, with signals from 0.8 V below V_{DD} to 1.2 V above V_{SS}, the channel protector behaves like a series resistor (typically 60 Ω), with leakage of about 1 nA. But when the applied voltage goes above V_{DD} or below V_{SS}—even with 0 supply voltage (power off)—one of the MOSFETs will switch off, opening the input circuit and clamping the output.



Because the channel protection works whether the supplies are present or not, and no control logic is required, these devices are ideal for use in applications where correct power sequencing cannot always be guaranteed (for example, hot-insertion rack systems).

Operating temperature range is –40 to +85°C. The ADG466 is available in 8-pin DIP, SOIC, and µSOIC; the ADG467 is available in 18-pin SOIC and 20-pin SSOP. ADG466/467 prices (1000) are $1.25/$2.15.

Faxcode* 2067 or Circle 18 A

Regulated Switched-Cap V Converter

ADP3603 provides –3.0 V, up to 50 mA, 3% accuracySwitches at 120 kHz; no inductors, small capacitors

The ADP3603 is a high-accuracy switched-capacitor voltage converter operating at a 120-kHz switching frequency, generated by an internal 240-kHz clock. It accepts +5-V dc input and furnishes up to 50 mA at a regulated –3.0 V (±3%). The ADP3603 is a lower-power (and -cost) version of the 120-mA ADP3604, described in *Analog Dialogue* 30-3 (p. 19, also p. 14, this issue).

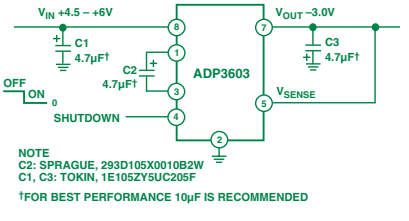
The ADP3603 is primarily designed for use as a negative-voltage regulator/inverter, allowing a single battery or system supply to suffice in applications calling for its positive voltage to be supplemented locally with negative voltage.

The operating principle is simple: a "pump" capacitor is switched between the input circuit and the output circuit, transferring increments of charge from an input storage capacitor to the output storage capacitor. Voltage inversion is achieved by reversing the switch connections to the output capacitor. No inductors are necessary.

Typical areas of application include general-purpose voltage inversion and regulation, computer peripherals and add-on cards, portable instruments, battery-powered devices, pagers and radio control receivers, disk drives, and mobile phones.

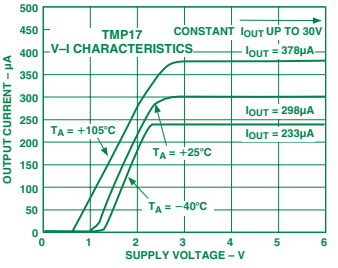
The AD3603 is housed in an 8-pin SO package and operates from –40 to +85°C. An evaluation board is available. AD3603 is priced at $1.70 in 1000s.

Faxcode* 1982 or Circle 20 A



Temperature Sensor

2-terminal TMP17 in SO-8 1 µA/K PTAT output current



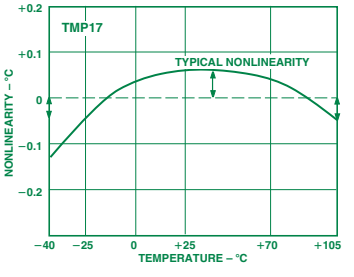
The TMP17 is a monolithic temperature-to-current transducer that provides an output current proportional to absolute temperature (PTAT), 1 microampere per kelvin, for temperatures from –40 to +105°C (233 to 378 K). Current is independent of applied voltage, for supplies from +4 to +30 V.

The device is inherently linear (within 0.5°C) and stable (repeatability and long-term stability within 0.2°C), and initial calibration error (25°C) is ±2.5°C max (F grade). Initial calibration error can be trimmed out by adjusting the measuring resistance that converts current to voltage.

Because the TMP17 is a current source, its output is immune to voltage noise pickup and IR drops in the signal leads in remote applications. The TMP17's small size, low cost, stability, and simplicity make it useful in applications such as cold-junction compensation, thermal compensation of instrumentation, and over-temperature warning systems in automotive, HVAC, and industrial temperature control.

The TMP17 is housed in a tiny SO-8 package and available in F and G grades. Prices in 1000s are $2.28 and $1.52.

Faxcode* 2040 or Circle 19 A



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Ask The Applications Engineer—23

by Erik Barnes

CURRENT FEEDBACK AMPLIFIERS—II

Part I (*Analog Dialogue* 30-3) covers basic operation of the current-feedback (CF) op-amp. This second part addresses frequently asked questions about common applications.

Q. I now have better understanding of how a current feedback op-amp works, but I'm still confused when it comes to applying one in a circuit. Does the low inverting input impedance mean I can't use the inverting gain configuration?

A. Remember that the inverting mode of operation works *because* of the low-impedance node created at the inverting input. The summing junction of a voltage-feedback (VF) amplifier is characterized by a low input impedance after the feedback loop has settled. A current feedback op amp will, in fact, operate very well in the inverting configuration because of its inherently low inverting-input impedance, holding the summing node at "ground," even before the feedback loop has settled. CF types don't have the voltage spikes that occur at the summing node of voltage feedback op amps in high-speed applications. You may also recall that advantages of the inverting configuration include maximizing input slew rate and reducing thermal settling errors.

Q. So this means I can use a current feedback op amp as a current-to-voltage converter, right?

A. Yes, they can be configured as I-to-V converters. But there are limitations: the amplifier's bandwidth varies directly with the value of feedback resistance, and the inverting input current noise tends to be quite high. When amplifying low level currents, higher feedback resistance means higher signal-to-(resistor-) noise ratio, because signal gain will increase proportionally, while resistor noise goes as $\sqrt{R}$. Doubling the feedback resistance doubles the signal gain and increases resistor noise by a only factor of 1.4; unfortunately the contribution from current noise is doubled, and, with a current feedback op amp, the signal bandwidth is halved. Thus the higher current noise of CF op amps may preclude their use in many photodiode-type applications. When noise is less critical, select the feedback resistor based on bandwidth requirements; use a second stage to add gain.

Q. I did notice the current noise is rather high in current feedback amplifiers. So will this limit the applications in which I can use them?

A. Yes, the inverting input current noise tends to be higher in CF op amps, around 20 to 30 pA/$\sqrt{\text{Hz}}$. However, the input voltage noise tends to be quite low when compared with similar voltage feedback parts, typically less than 2 nV/$\sqrt{\text{Hz}}$, and the feedback resistance will also be low, usually under 1 kΩ. At a gain of 1, the dominant source of noise will be the inverting-input noise current flowing through the feedback resistor. An input noise current of 20 pA/$\sqrt{\text{Hz}}$ and an R_F of 750 Ω yields 15 nV/$\sqrt{\text{Hz}}$ as the dominant noise source at the output. But as the gain of the circuit is increased (by reducing input resistance), the output noise due to input current noise will not increase, and the amplifier's input *voltage* noise will become the dominant factor. At a gain, of say, 10, the contribution from the input noise current is only 1.5 nV/$\sqrt{\text{Hz}}$ when referred to the input; added to the input voltage noise of the amplifier in RSS fashion, this gives an input-referred noise voltage of only 2.5 nV/$\sqrt{\text{Hz}}$ (neglecting resistor noise). Used thus, the CF op amp becomes attractive for a low noise application.

Q. What about using the classic four-resistor differential configuration? Aren't the two inputs unbalanced and therefore not suitable for this type of circuit?

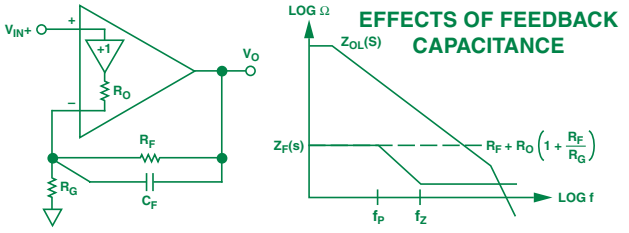
A. I'm glad you asked; this is a common misconception of CF op amps. True, the inputs are not matched, but the transfer function for the ideal difference amplifier will still work out the same. What about the unbalanced inputs? At lower frequencies, the four-resistor differential amplifier's CMR is limited by the matching of the external resistor ratios, with 0.1% matching yielding about 66 dB. At higher frequencies, what matters is the matching of time constants formed by the input impedances. High-speed voltage-feedback op amps usually have pretty well matched input capacitances, achieving CMR of about 60 dB at 1 MHz. Because the CF amplifier's input stage is unbalanced, the capacitances may not be well matched. This means that small external resistors (100 to 200 Ω) must be used on the noninverting input of some amplifiers to minimize the mismatch in time constants. If careful attention is given to resistor selection, a CF op amp can yield high frequency CMR comparable to a VF op amp. Both VF and CF amplifiers can further benefit from additional hand-trimmed capacitors at the expense of signal bandwidth. If higher performance is needed, the best choice would be a monolithic high speed *difference amplifier*, such as the AD830. Requiring no resistor matching, it has a CMR > 75 dB at 1 MHz and about 53 dB at 10 MHz.

Q. What about trimming the amplifier's bandwidth with a feedback capacitor? Will the low impedance at the inverting input make the current feedback op amp less sensitive to shunt capacitance at this node? How about capacitive loads?

A. First consider a capacitor in the feedback path. With a voltage feedback op amp, a pole is created in the noise gain, but a pole and a zero occur in the feedback transresistance of a current feedback op amp, as shown in the figure below. Remember that the phase margin at the intersection of the feedback transresistance and the open loop transimpedance will determine closed-loop stability. Feedback transresistance for a capacitance, C_F, in parallel with R_F, is given by

$$Z_F(s)=\left[R_F+R_O\left(1+\frac{R_F}{R_G}\right)\right]\frac{1+\dfrac{sC_FR_FR_GR_O}{R_FR_G+R_FR_O+R_GR_O}}{1+sC_FR_F}$$

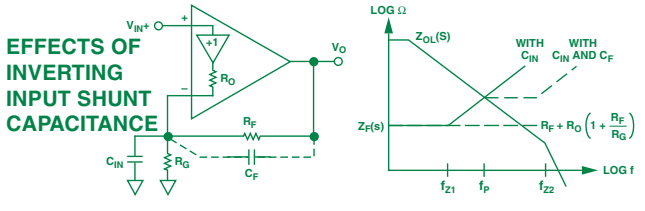
The pole occurs at $1/2\pi R_FC_F$, and the zero occurs higher in frequency at $1/[2\pi(R_F||R_G||R_O)C_F]$. If the intersection of Z_F and Z_{OL} occurs too high in frequency, instability may result from excessive open loop phase shift. If $R_F \rightarrow \infty$, as with an integrator circuit, the pole occurs at a low frequency and very little resistance exists at higher frequencies to limit the loop gain. A CF integrator can be stabilized by a resistor in series with the integrating capacitor to limit loop gain at higher frequencies. Filter topologies that use reactive feedback, such as multiple feedback types, are not suitable for CF op amps; but Sallen-Key filters, where the op amp is used as a fixed-gain block, are feasible. In general, it is not desirable to add capacitance across R_F of a CF op amp.



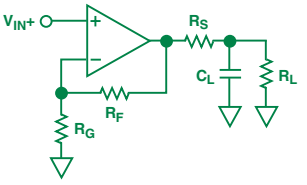
Another issue to consider is the effect of shunt capacitance at the inverting input. Recall that with a voltage feedback amplifier, such capacitance creates a zero in the noise gain, increasing the rate of closure between the noise gain and open loop gain, generating excessive phase shift that can lead to instability if not compensated for. The same effect occurs with a current feedback op amp, but the problem may be less pronounced. Writing the expression for the feedback transresistance with the addition of C_{IN}:

$$Z_F(s) = \left[R_F + R_O\left(1 + \frac{R_F}{R_G}\right)\right]\left[1 + \frac{sC_{IN}R_FR_GR_O}{R_FR_G + R_FR_O + R_GR_O}\right]$$

A zero occurs at $1/[2\pi(R_F||R_G||R_O)C_{IN}]$, shown in the next figure (f_{Z1}). This zero will cause the same trouble as with a VF amplifier, but the corner frequency of the zero tends to be higher in frequency because of the inherently low input impedance at the inverting input. Consider a wideband voltage feedback op amp with R_F = 750 Ω, R_G = 750 Ω, and C_{IN} = 10 pF. The zero occurs at $1/[2\pi(R_H||R_G)C_{IN}]$, roughly 40 MHz, while a current feedback op-amp in the same configuration with an R_O of 40 Ω will push the zero out to about 400 MHz. Assuming a unity gain bandwidth of 500 MHz for both amplifiers, the VF amplifier will require a feedback capacitor for compensation, reducing the effect of C_{IN}, but also reducing the signal bandwidth. The CF device will certainly see some additional phase shift from the zero, but not as much because the break point is a decade higher in frequency. Signal bandwidth will be greater, and compensation may only be necessary if in-band flatness or optimum pulse response is required. The response can be tweaked by adding a small capacitor in parallel with R_F to reduce the rate of closure between Z_F and Z_{OL}. To ensure at least 45° of phase margin, the feedback capacitor should be chosen to place a pole in the feedback transresistance where the intersection of Z_F and Z_{OL} occurs, shown here (f_P). Don't forget the effects of the higher frequency zero due to the feedback capacitor (f_{Z2}).



Load capacitance presents the same problem with a current feedback amplifier as it does with a voltage feedback amplifier: increased phase shift of the error signal, resulting in degradation of phase margin and possible instability. There are several well-documented circuit techniques for dealing with capacitive loads, but the most popular for high speed amplifiers is a resistor in series with the output of the amplifier (as shown below). With the resistor outside the feedback loop, but in series with the load capacitance, the amplifier doesn't directly drive a purely capacitive load. A CF op amp also gives the option of increasing R_F to reduce the loop gain. Regardless of the approach taken, there will always be a penalty in bandwidth, slew rate, and settling time. It's best to experimentally optimize a particular amplifier circuit, depending on the desired characteristics, e.g., fastest rise time, fastest settling to a specified accuracy, minimum overshoot, or passband flatness.



Q. Why don't any of your current feedback amplifiers offer true single-supply operation, allowing signal swings to one or both rails?

A. This is one area where the VF topology is still favored for several reasons. Amplifiers designed to deliver good current drive and to swing close to the rails usually use common-emitter output stages, rather than the usual emitter followers. Common emitters allow the output to swing to the supply rail minus the output transistors' V_{CE} saturation voltage. With a given fabrication process, this type of output stage does not offer as much speed as emitter followers, due in part to the increased circuit complexity and inherently higher output impedance. Because CF op amps are specifically developed for the highest speed and output current, they feature emitter follower output stages.

With higher speed processes, such as ADI's XFCB (extra-fast complementary bipolar), it has been possible to design a common-emitter output stage with 160-MHz bandwidth and 160-V/µs slew rate, powered from a single 5-volt supply (AD8041). The amplifier uses voltage feedback, but even if, somehow, current feedback had been used, speed would still be limited by the output stage. Other XFCB amplifiers, with emitter-follower output stages (VF or CF), are much faster than the AD8041. In addition, single-supply input stages use PNP differential pairs to allow the common-mode input range to extend down to the lower supply rail (usually ground). To design such an input stage for CF is a major challenge, not yet met at this writing.

Nevertheless, CF op amps can be used in single-supply applications. Analog Devices offers many amplifiers that are specified for +5- or even +3-volt operation. What must be kept in mind is that the parts operate well off a single supply *if the application remains within the allowable input and output voltage ranges*. This calls for level shifting or ac coupling and biasing to the proper range, but this is already a requirement in most single-supply systems. If the system must operate to one or both rails, or if the maximum amount of headroom is demanded in ac-coupled applications, a current feedback op amp may simply not be the best choice. Another factor is the rail-to-rail output swing specifications when driving heavy loads. Many so-called rail-to-rail parts don't even come close to the rails when driving back- terminated 50- or 75-Ω cables, because of the increase in V_{CESAT} as output current increases. If you really need true rail-to-rail performance, you don't want or need a current feedback op amp; if you need highest speed and output current, this is where CF op amps excel. A

Worth Reading

NEW DATABOOK

Designer's Reference Manual [1996] Contains more than 1100 pages of data, including selection trees, selection guides, and two-page data sheets on more than 438 generic product types. [Multi-page data sheets, with more-detailed data on individual products, are available via Faxcodes, the Internet, a CD-ROM, or phone calls or faxes to ADI's Literature Distribution Center.] **FREE—Circle 21**

SERIALS

DSPatch—The DSP Applications Newsletter: Number 36 (Fall, 1996, 16 pages) features the low-cost ADSP-2104 and performance/cost improvements to other family members; use of ADSP-2101 in Doppler traffic safety radar; a SHARC-based FM broadcast radio exciter. Also, program code and data overlays in ADSP-2181-based DSP systems; interfacing SHARC DSPs to flash memory; four articles about third-party users; tips on writing a C program for a SHARC DSP. Plus Q&A, Update, and much more. **FREE, Circle 22**

COMMUNICATIONS DIRECT—Systems and IC solutions for demanding markets: Volume 2, No. 1 (August, 1996, 8 pages). Features articles on GSM, chipsets, and the type approval process. And more... **FREE, Circle 23**

Accelerometer News, Issue 5 (October, 1996, 4 pages). Features the ADXL150 and ADXL250 single- and dual-axis 50-*g* accelerometers with 10-m*g* resolution; a vibration-cutoff switch design; an interesting series of acceleration waveforms; and news about ADI's new dedicated fab for micromachined products in Cambridge, MA. **FREE, Circle 24**

ANALOG BRIEFINGS—The newsletter for the defense/aerospace industries, Volume 11, No. 1 (October, 1996, 8 pages). Features new-product introductions and discussions of: the integral EMI filter for conducted noise in ADI's new line of high-density dc-dc converters; ADI's recent worldwide QML certification; an upcoming Quad-SHARC module; product additions to ADI's RADTEST^{SM} database. **FREE, Circle 25**

Signals—Issue 3 (October, 1996, 4 pages). Features articles on signal-conditioning modules, boards, and accessories available from Analog Devices, including the 5B, 6B, and 7B module series, and RTI-2100 series boards and multiplexer panels. **FREE, Circle 26**

BROCHURES AND GUIDES

The Analog Devices family of Instrumentation Amplifiers, a 6-page guide to selecting IC instrumentation amplifiers. Includes 5 new members, the low-cost AD620, AD621, AD622 and the single-supply AD626 and AMP04. **Circle 27**

Quick Reference Guide: Industrial signal conditioning and data acquisition I/O solutions, a 6-page brief guide to the 2B, 3B, 5B, 6B, and 7B series of signal conditioning modules and the RTI family of data-acquisition boards. **FREE, Circle 28**

PRODUCT HIGHLIGHT BRIEF BROCHURE

AD20msp910 ADSL Chipset: Lowest-cost, most-complete solution for ADSL Modems, including all required hardware and software components for an ADSL transceiver and host processor. **Circle 29**

APPLICATION NOTES

Interfacing the AD22100 temperature sensor to a low-cost single-chip microcontroller, by Norm Bernstein [12 pp., AN-395]. The AD22100 (*Analog Dialogue* 29-1, 1995) is a monolithic self-contained linear RTD and amplifier. The output of the AD22100 is proportional to supply voltage as well as temperature, so it can share a common reference with an A/D converter to minimize reference-related measurement errors ratiometrically. This Application Note discusses both hardware and software issues in a design employing an 80C51 microcontroller for A/D conversion. **Circle 30**

Fast rail-to-rail operational amplifiers ease design constraints in low-voltage high-speed systems, by Eamon Nash [8 pp., AN-417]. A discussion of output stages in rail-to-rail op amps, and several applications: driving high-speed ADCs; line drivers; active filters; transformer drive circuits; HDSL transceiver. **Circle 31**

A discrete, low-phase-noise, 125-MHz crystal oscillator for the AD9850 complete direct-digital synthesizer, by Richard Cushing (Analog Devices) and Steven Swift (Novatech Instruments, Inc.) [2 pp. AN419]. Solving the challenging problem of providing a clean, 125-MHz clock signal to exercise the AD9850 (*Analog Dialogue* 30-3, p. 12) at its fastest rate. **Circle 32** A

BOOK REVIEW

Electronic Communication Systems: A Complete Course, 2nd edition, by William Schweber. Englewood Cliffs, NJ: Prentice Hall, 1996. [not available from Analog Devices].

Bill Schweber, the author of this excellent 800-page textbook, is well-known to readers of *EDN* magazine (and earlier, to readers of *Analog Dialogue*). His writing is characterized by clarity of exposition and a practical approach. In the preface to the first edition, he set out his theme: to cover the traditional aspects of communications, yet recognize and explore three factors that have changed the face of communications systems: the widespread use of ICs to implement circuitry, the use of microprocessors and software to manage and improve the operation of traditional analog communication systems, and the use of digital techniques and signals to supplement or virtually replace analog techniques. The book provides a presentation of the way systems are commonly implemented, along with a discussion of the tradeoffs that exist in any system design: speed, power, performance, errors, complexity.

Over half the first edition was devoted to digital communications and actual communication systems—video, facsimile, telephone, modems, RS-232, cellular phones, computer networks, satellites, radar, fiber optics (following the necessary basic topics, such as bandwidth AM, FM, antennas, transmitters, receivers, and microwaves). The new edition has expanded its coverage into areas such as digital cellular phones, the numerous emerging standards for personal communication systems (mostly wireless), and wired and wireless networks including ISDN, SONET, ATM, and the Internet, along with discussions of the context in which they fit, and strengths and weaknesses. A

THE AUTHORS *(continued from page 2)*

Dave Robertson (page 11) is a design engineer in the Analog Devices High-Speed Converter group in Wilmington, MA. His photo and a brief biography appeared in *Analog Dialogue* 30-3.

Erik Barnes (page 20) is an Applications Engineer for ADI's High Speed Converter Group in Wilmington, MA. His photo and a brief biography appeared in *Analog Dialogue* 30-3. A

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NEW LITERATURE

Brochure: ***Signal processing components for automotive applications*** **Circle 33**

Product Briefs: ***GSM Baseband Chipset (AD20msp415)*** **and** ***Radio Transceiver Chipset (AD6430)*** **Circle 34**

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

IN THE LAST ISSUE

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ERRATA• • • Analog Dialogue 30-3, pages 10-11 ("Buffered multiplexers for video applications"): In **Figure 5, the two 700-Ω resistors at pins 7, 8 should be 549 Ω**; and the **grounded resistor should be connected to pin 7** instead of pin 8 **• • • AD7836 Quad 14-bit DAC data sheet**, Rev. 0: On the first page under "Features", The **reference range is ±5 V and the Maximum output voltage range is ±10 V • • • AD9830 data sheet** (CMOS complete DDS). **Rev. A, Outline Dimensions, page 15, has the correct values** for package pitch and pin width **(Circle 35)**. These are incorrect in Rev. 0 **• • •** The **AD7701 and AD7703 data sheets are in Revision D (Circle 36). Erroneous current consumption spec changes** from Rev. B to Rev. C **have been reversed.**

PRODUCT NOTES • • • The **correct version of AD7015** to order is **AD53/009-9 • • •** More than **200 products of all types, including DSPs and computer-oriented** products, are **available for single-supply applications**, especially useful in **power-saving 5- and 3-volt equipment**. Consult the sales/applications staff **• • • Nearly 300 ADI products are available with a maximum package thickness of 1.78 mm, suitable for PCM cards**, including DACs & ADCs, Op Amps & In Amps, References, DSPs, Drivers, Switches, and Codecs. Consult the sales/applications staff.

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